

FIG. 1

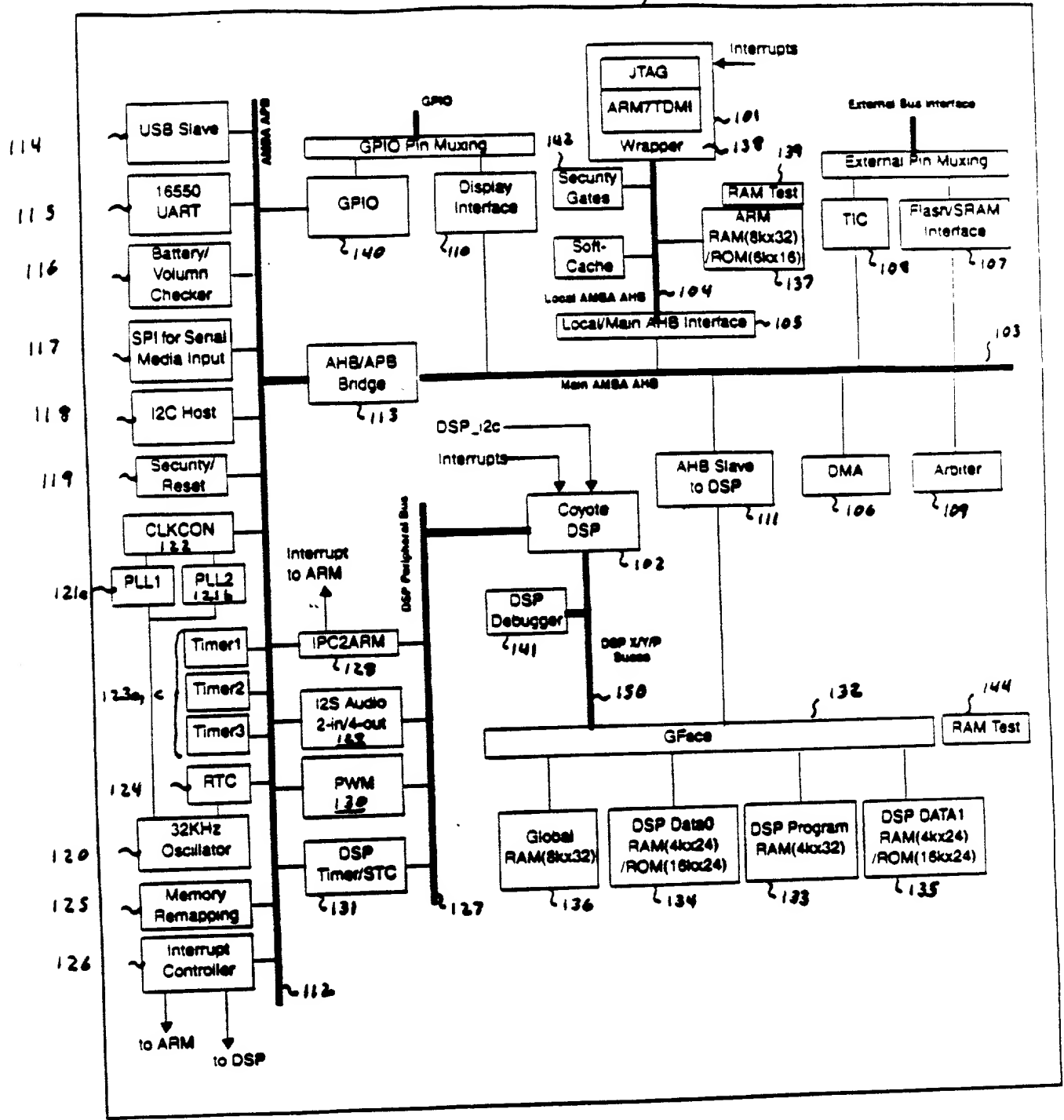
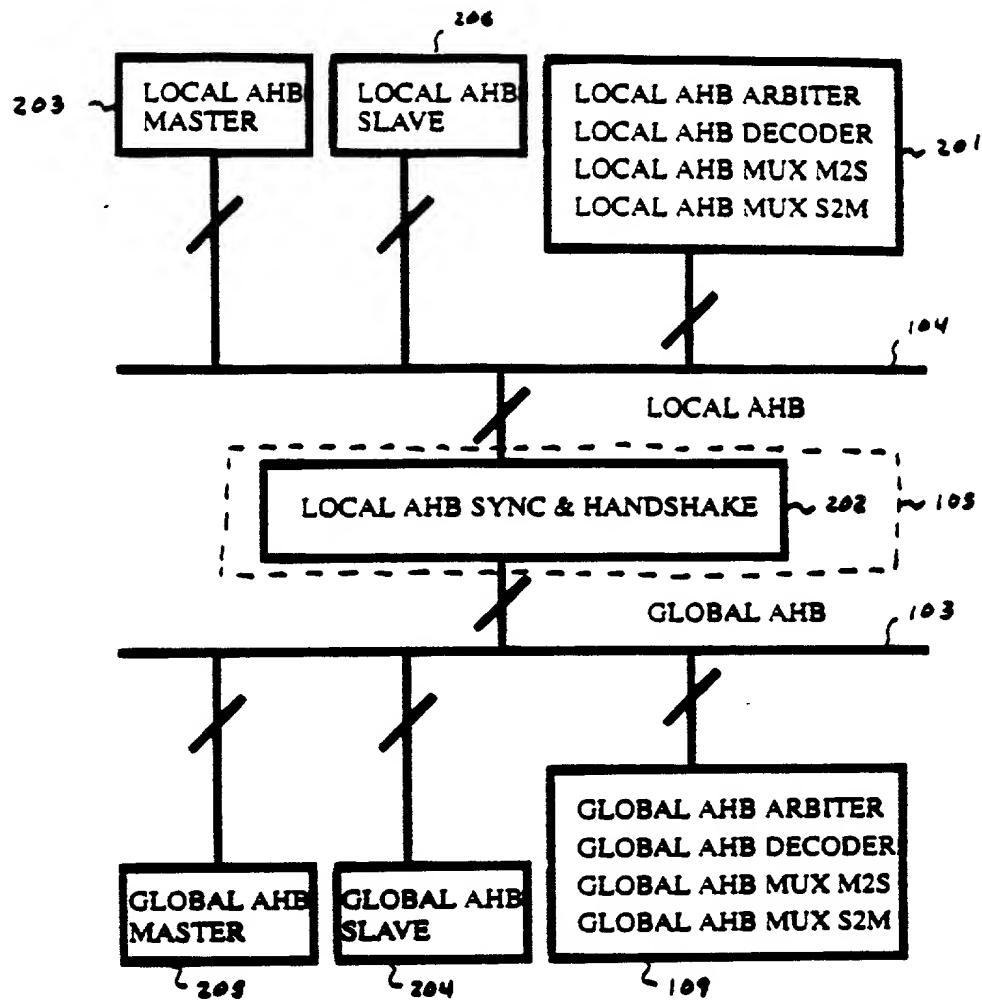


FIG. 2A



Address pushed in GHCLK domain

Data D(81) received in GHCLK domain

GHCLK

LHCLK

LHADDR

LHTRANS

LHREADY

LRDATA

LWDATA

GHADDR

GHREADY

GRDATA

GWDATA

GHSELaddrif

GHSELaddrif_reg

LHBUSREQaddrif

LHGRANT

FIG. 3B

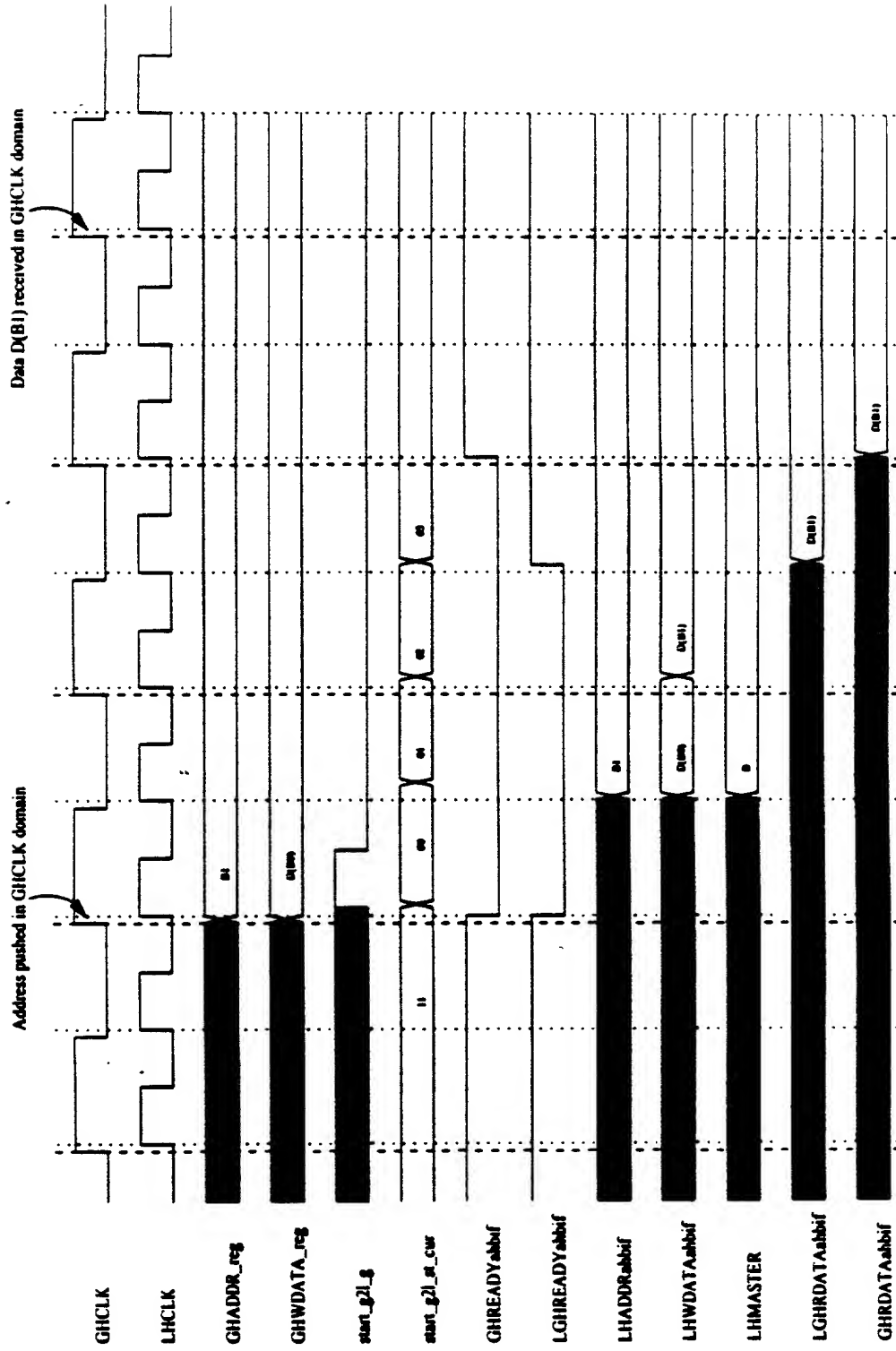


FIG 2C

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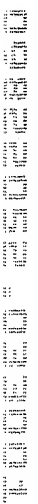


FIG. 4B

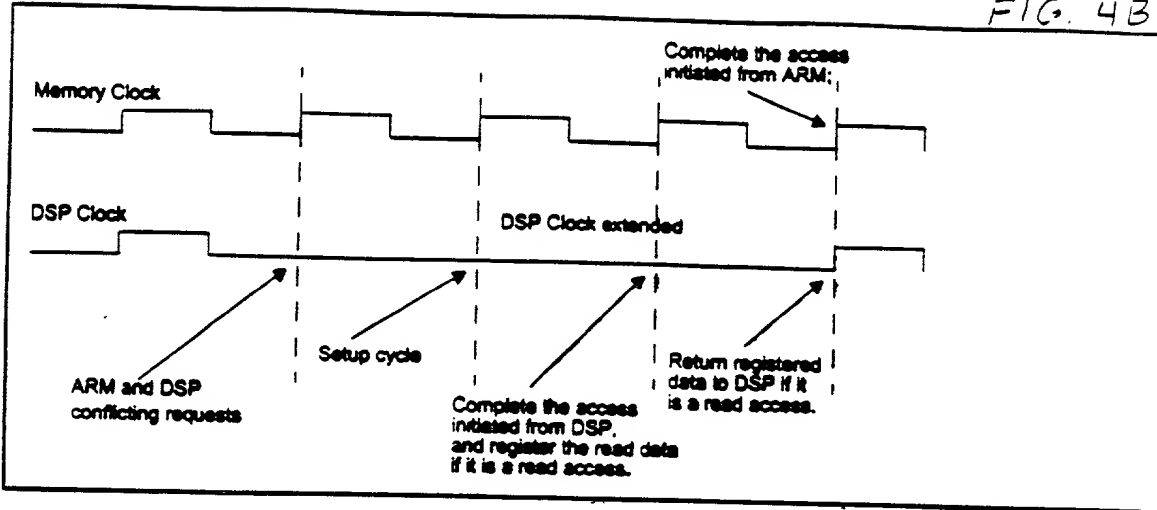
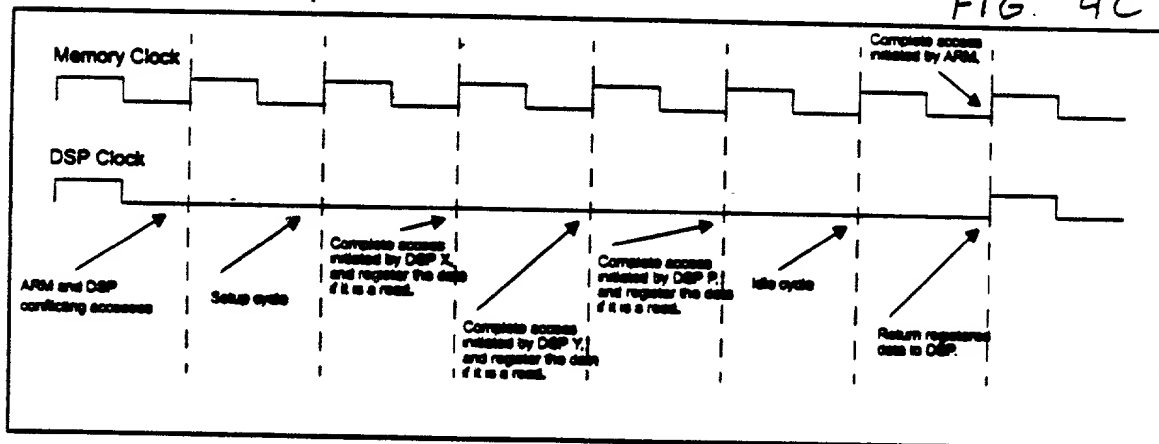
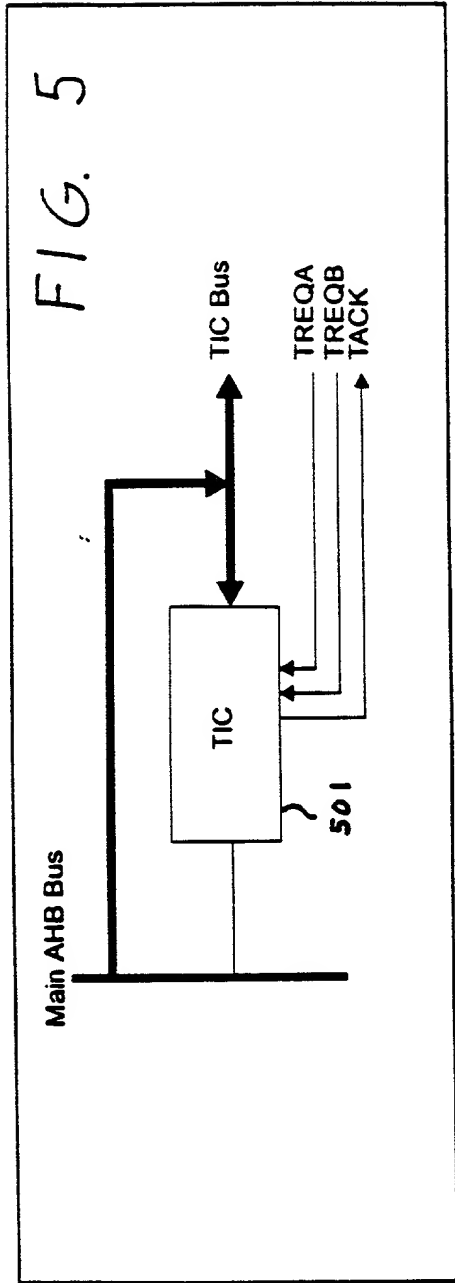
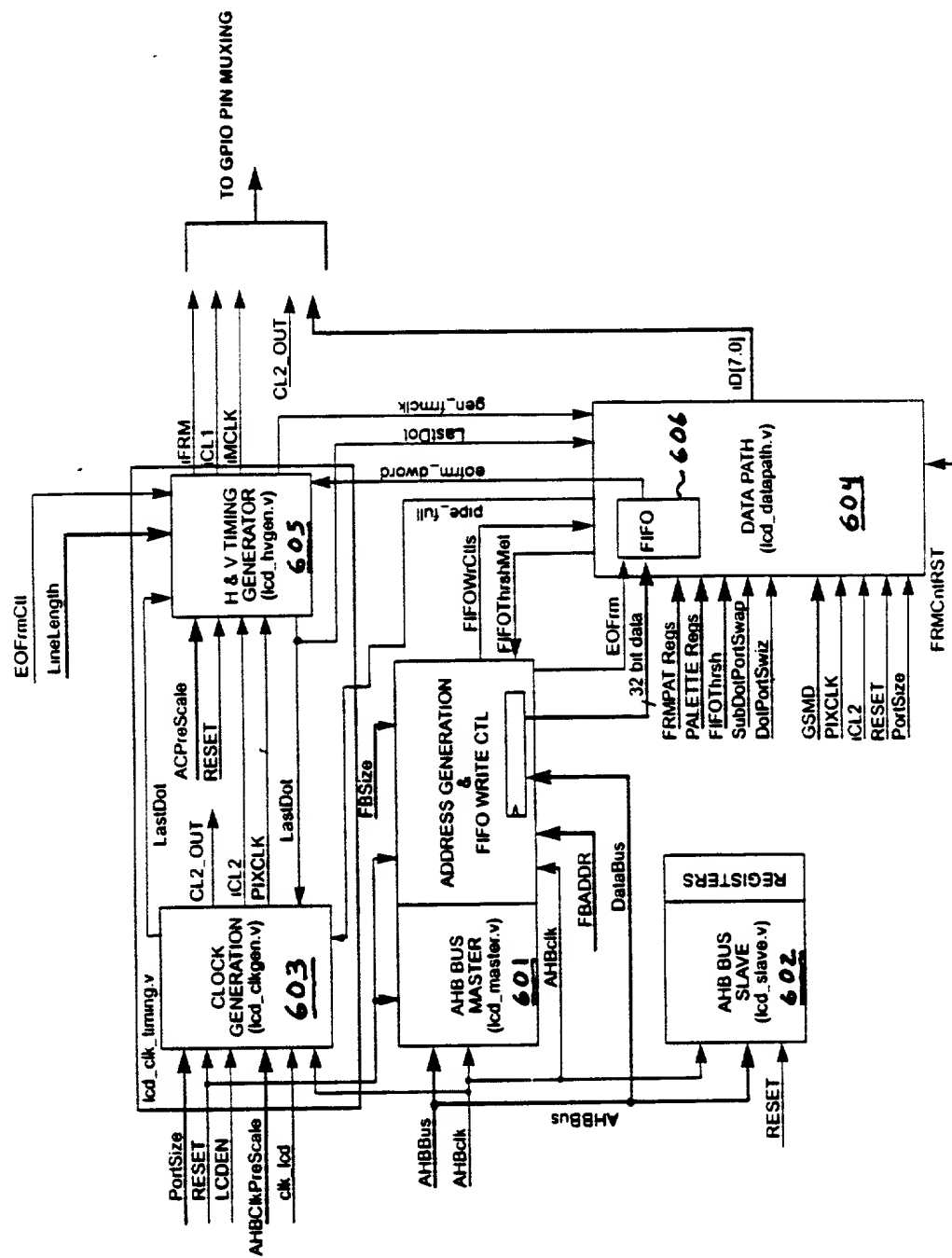


FIG. 4C







LCD Controller (lcd_top.v) Block Diagram

FIG. 6A

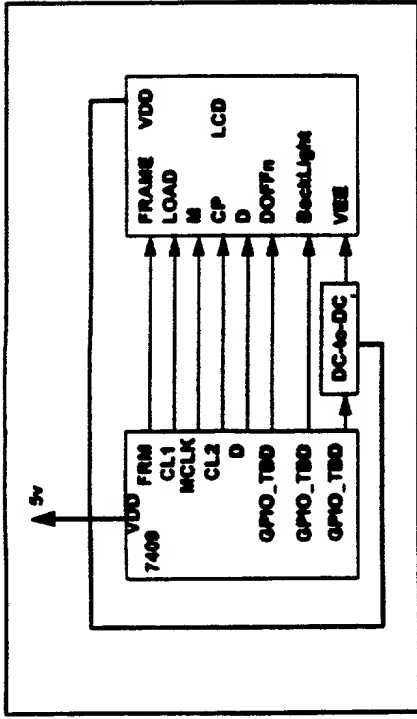


FIG 6B

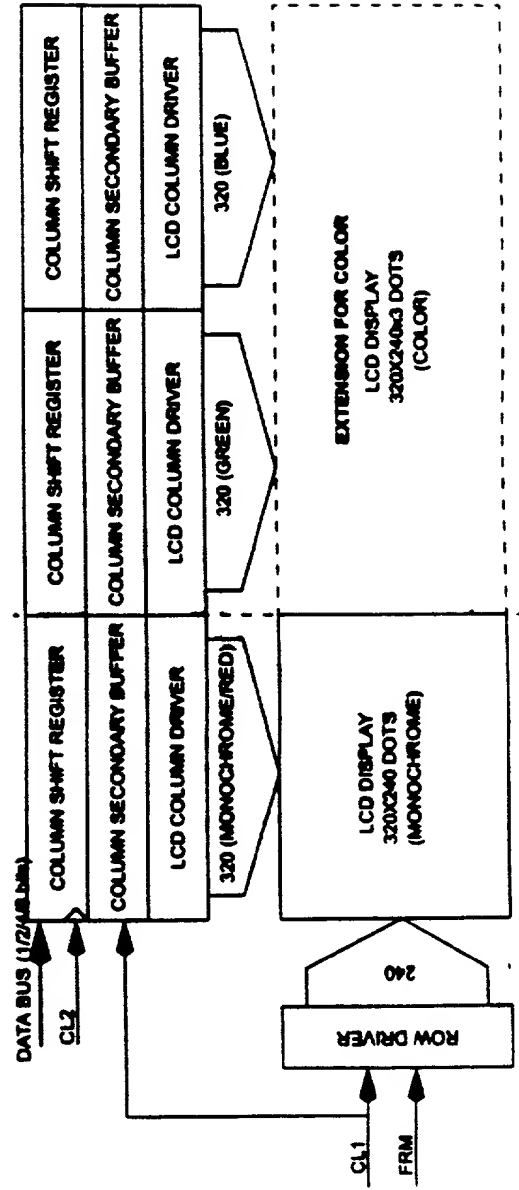


FIG 6C

FIG 6 E

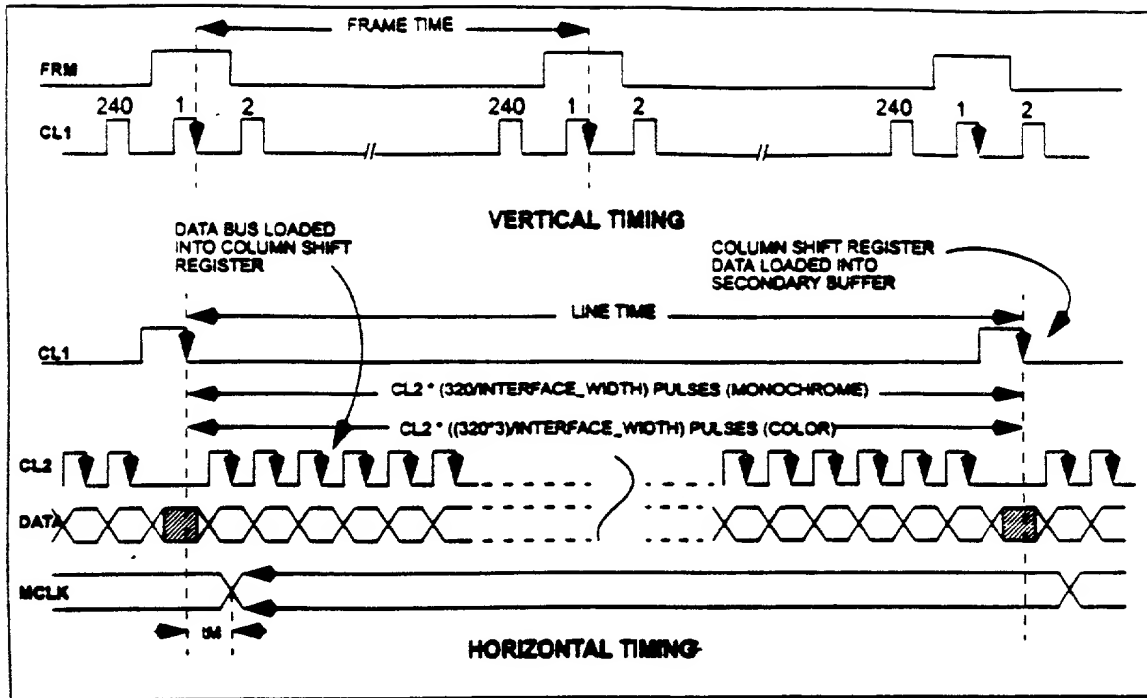


FIG 6 D

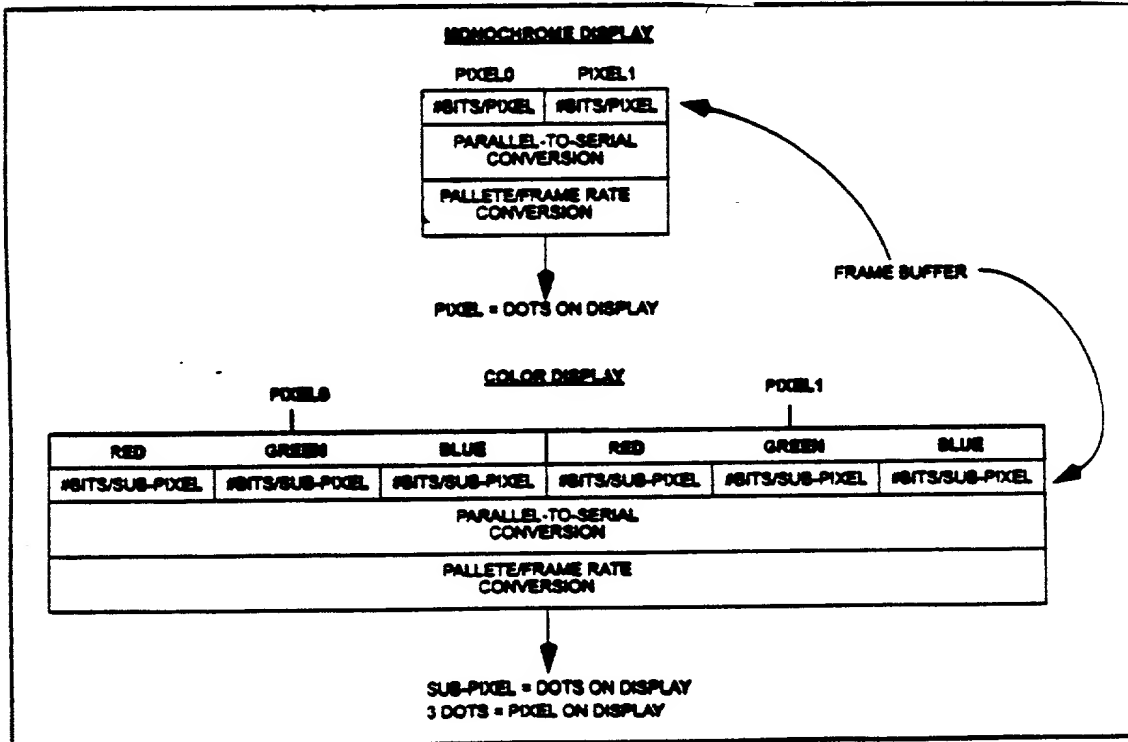


FIG 6G

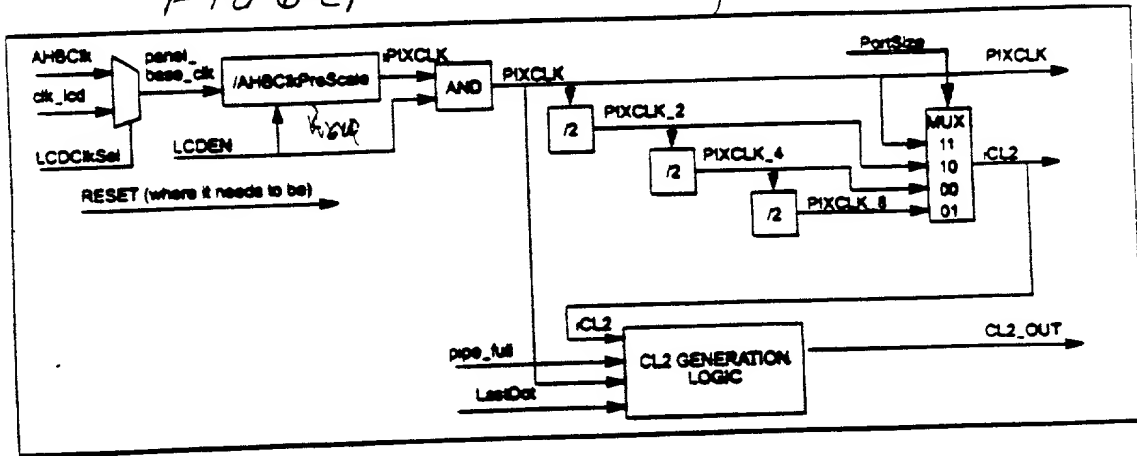
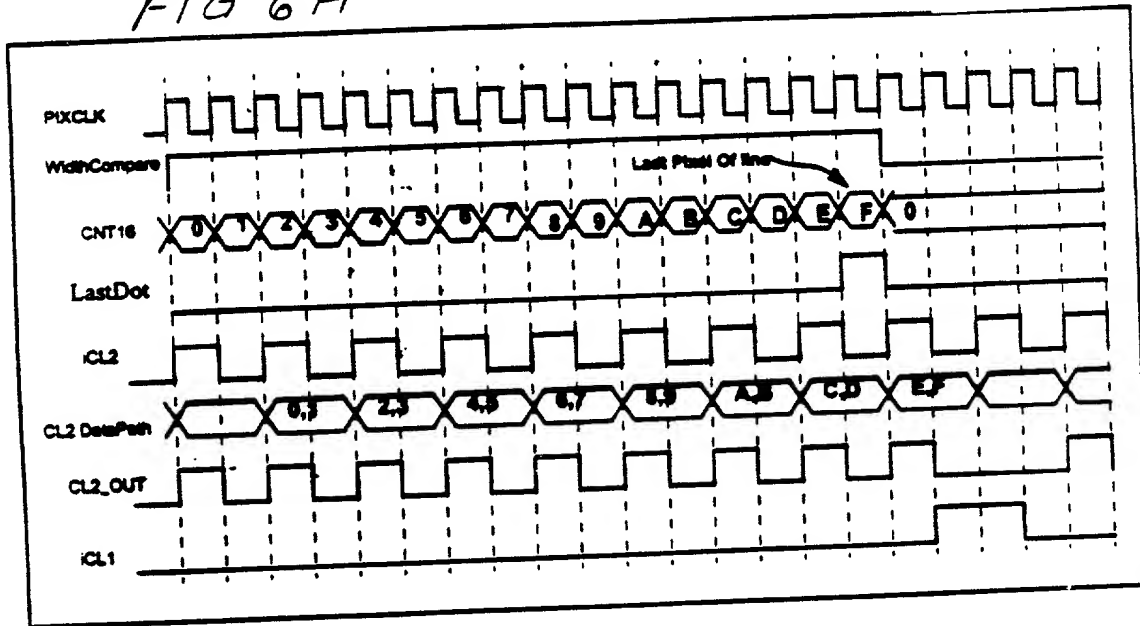


FIG 6H



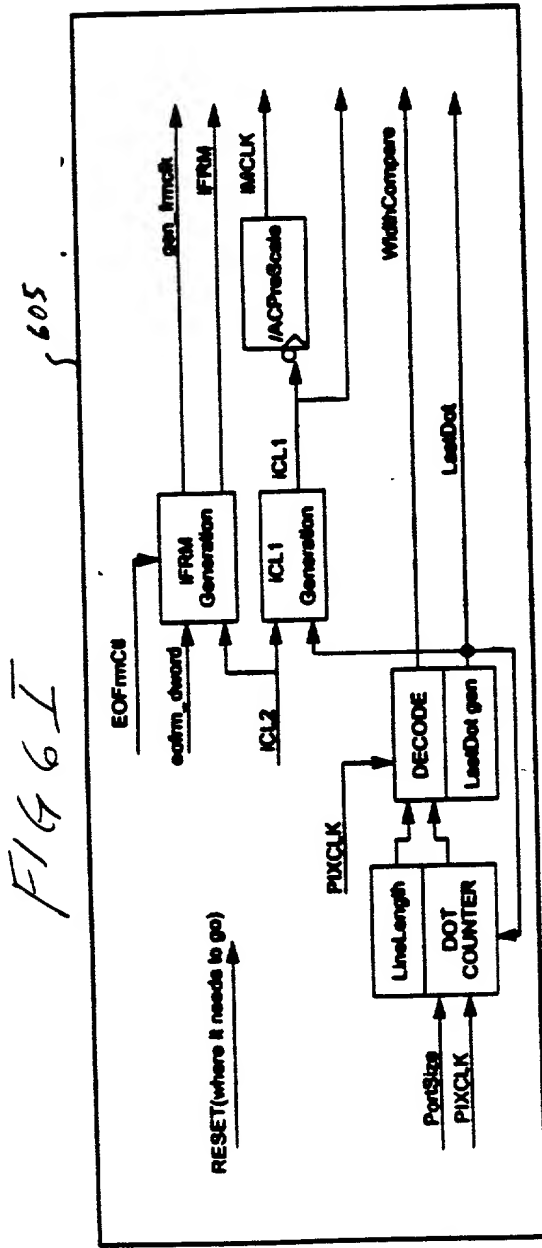


FIG 67

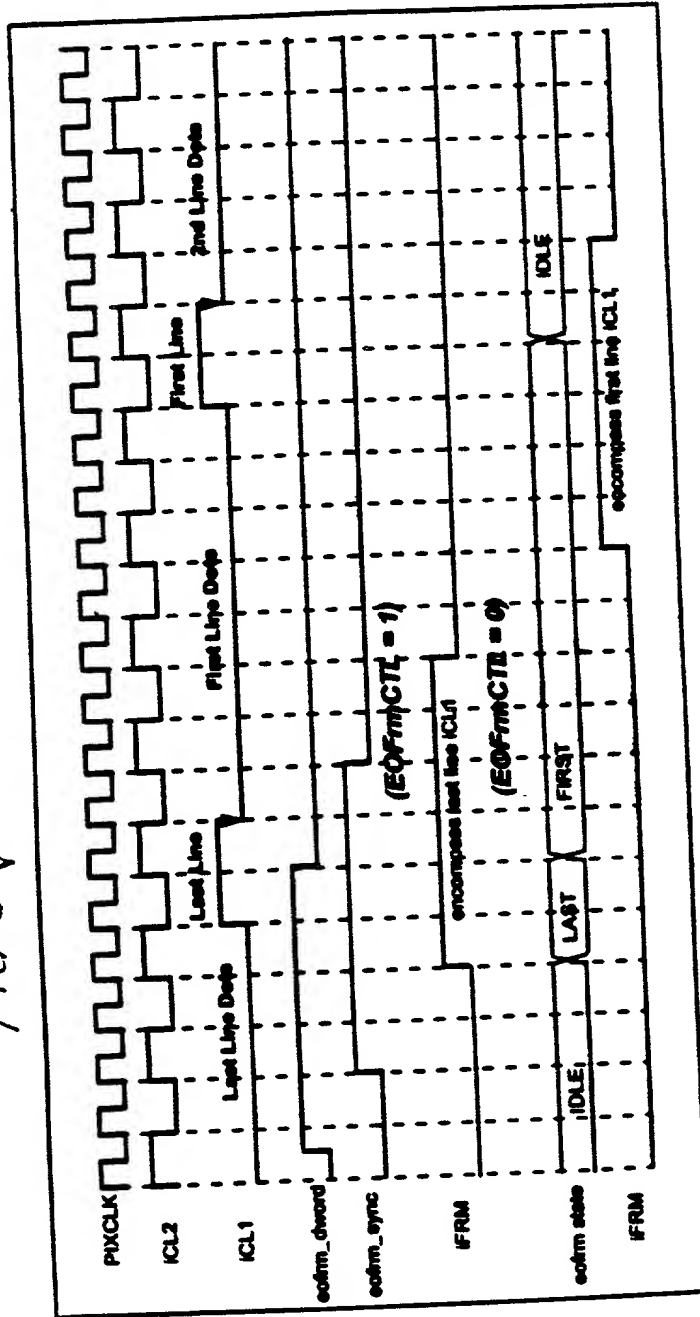


FIG. 6k

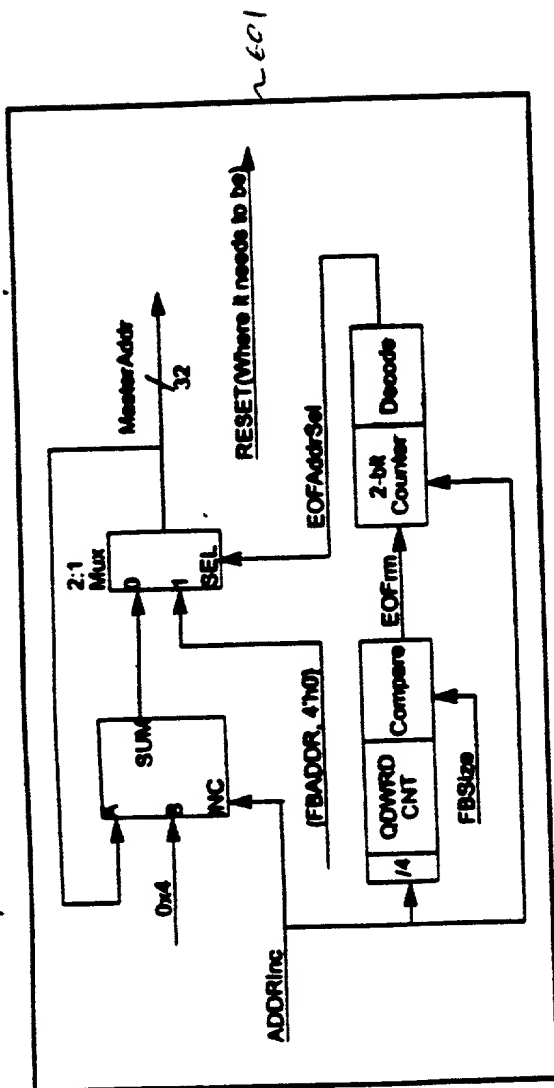


FIG 6L

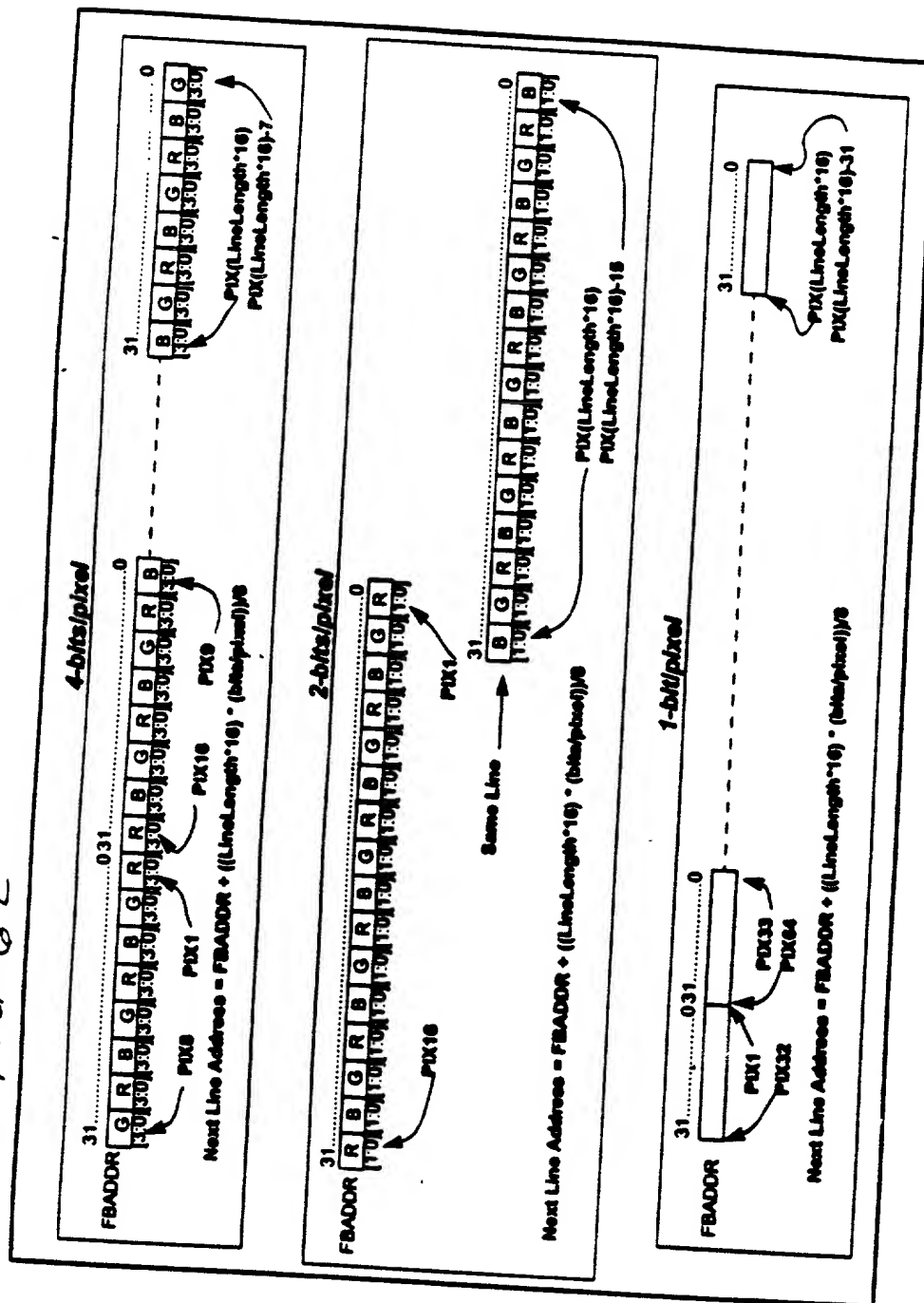


FIG 6M

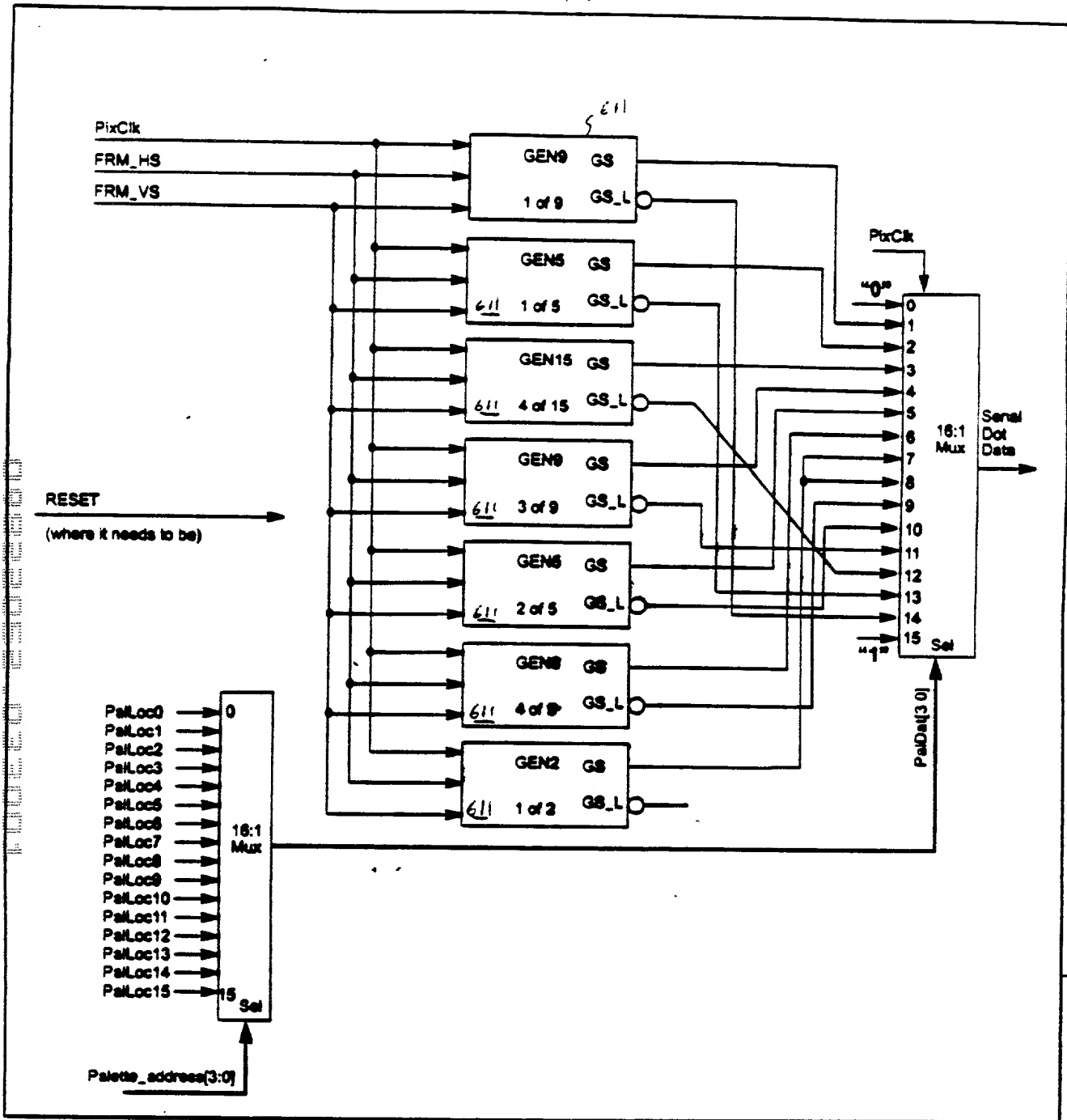
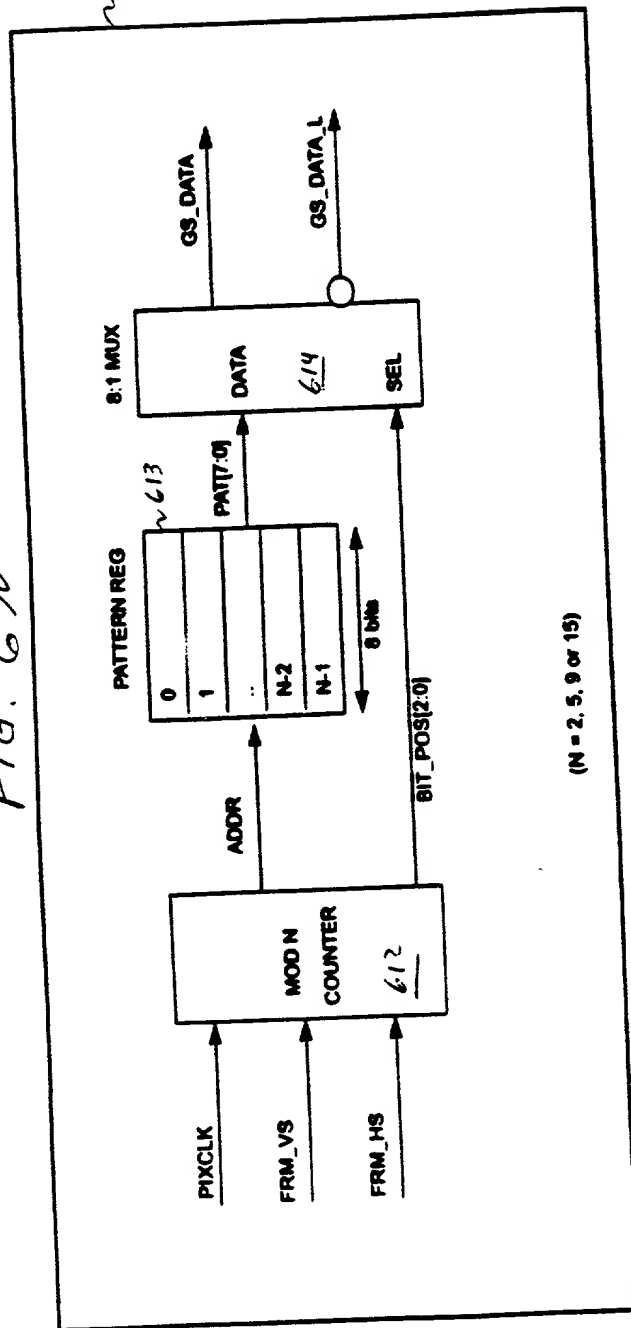


FIG. 6N



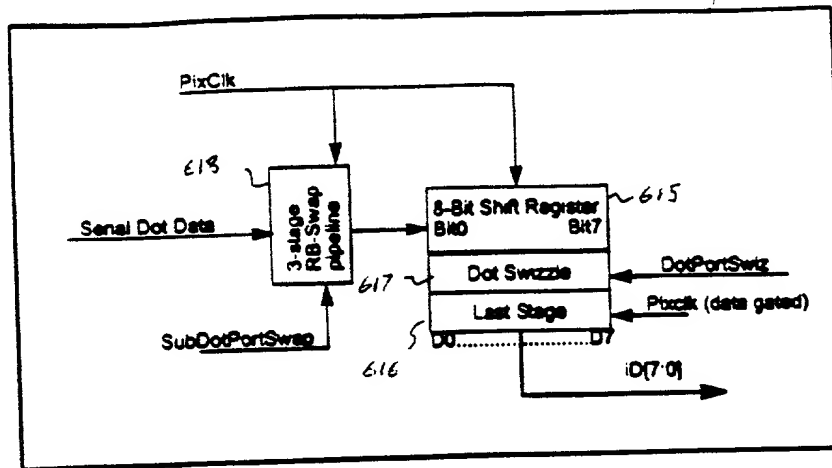
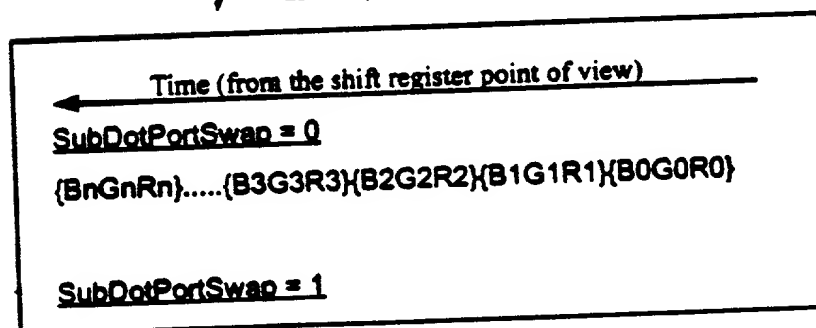


FIG 60

FIG. 6P



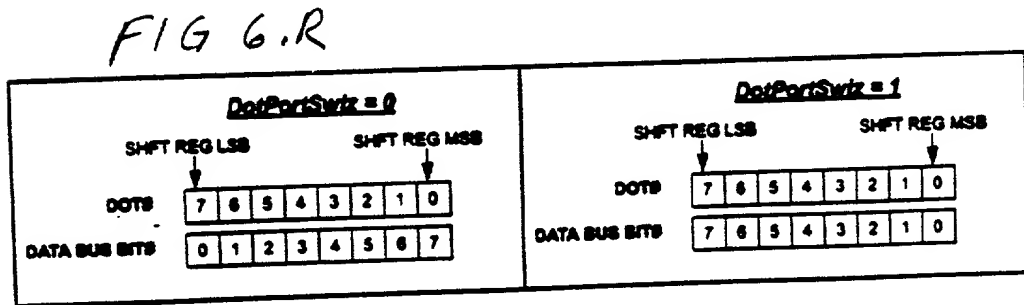
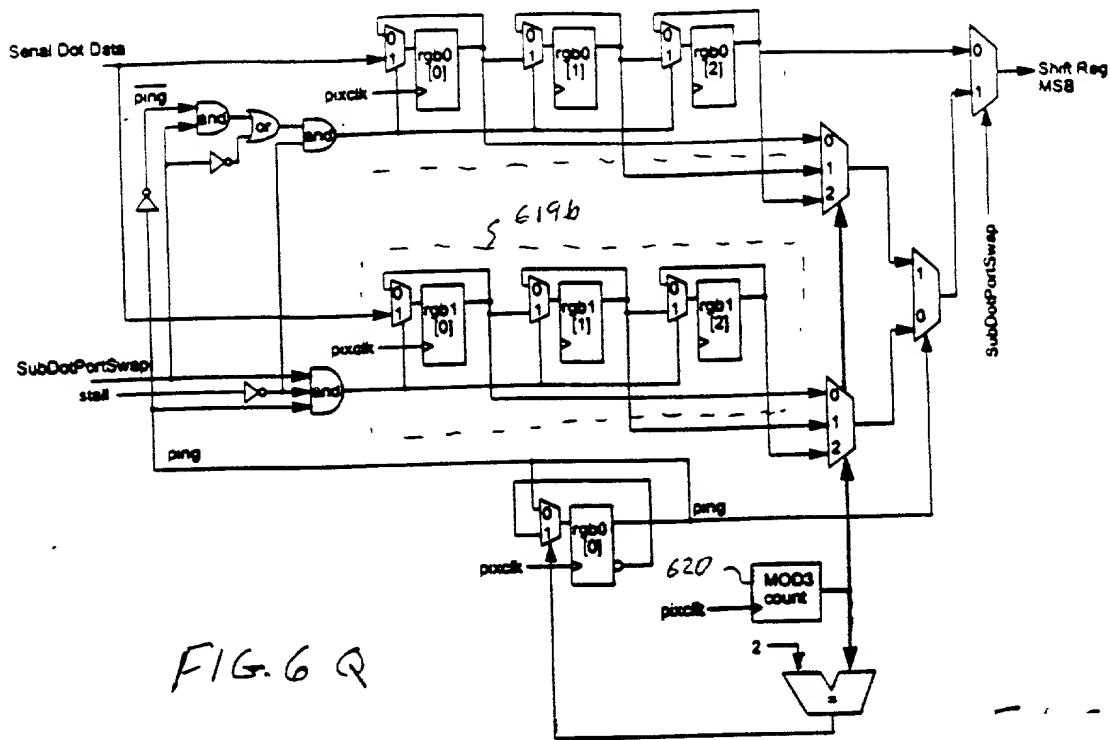
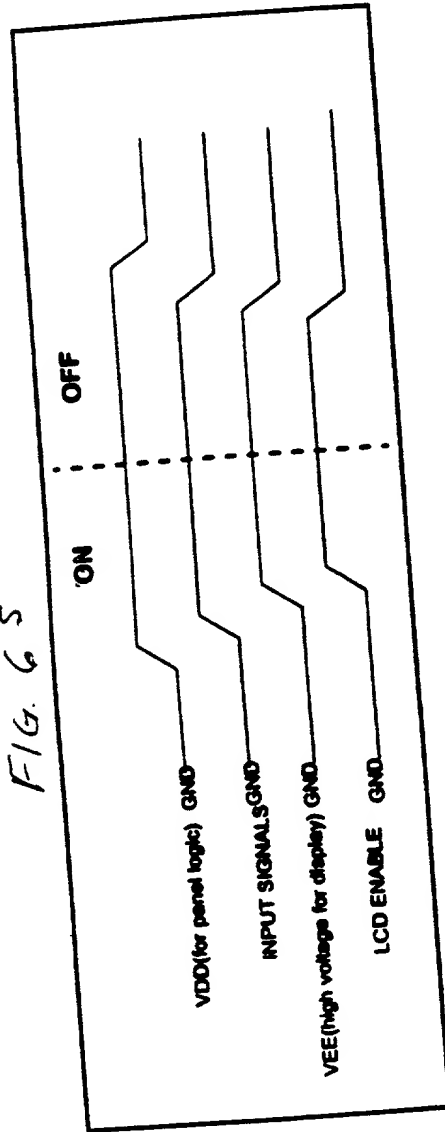


FIG. 6S



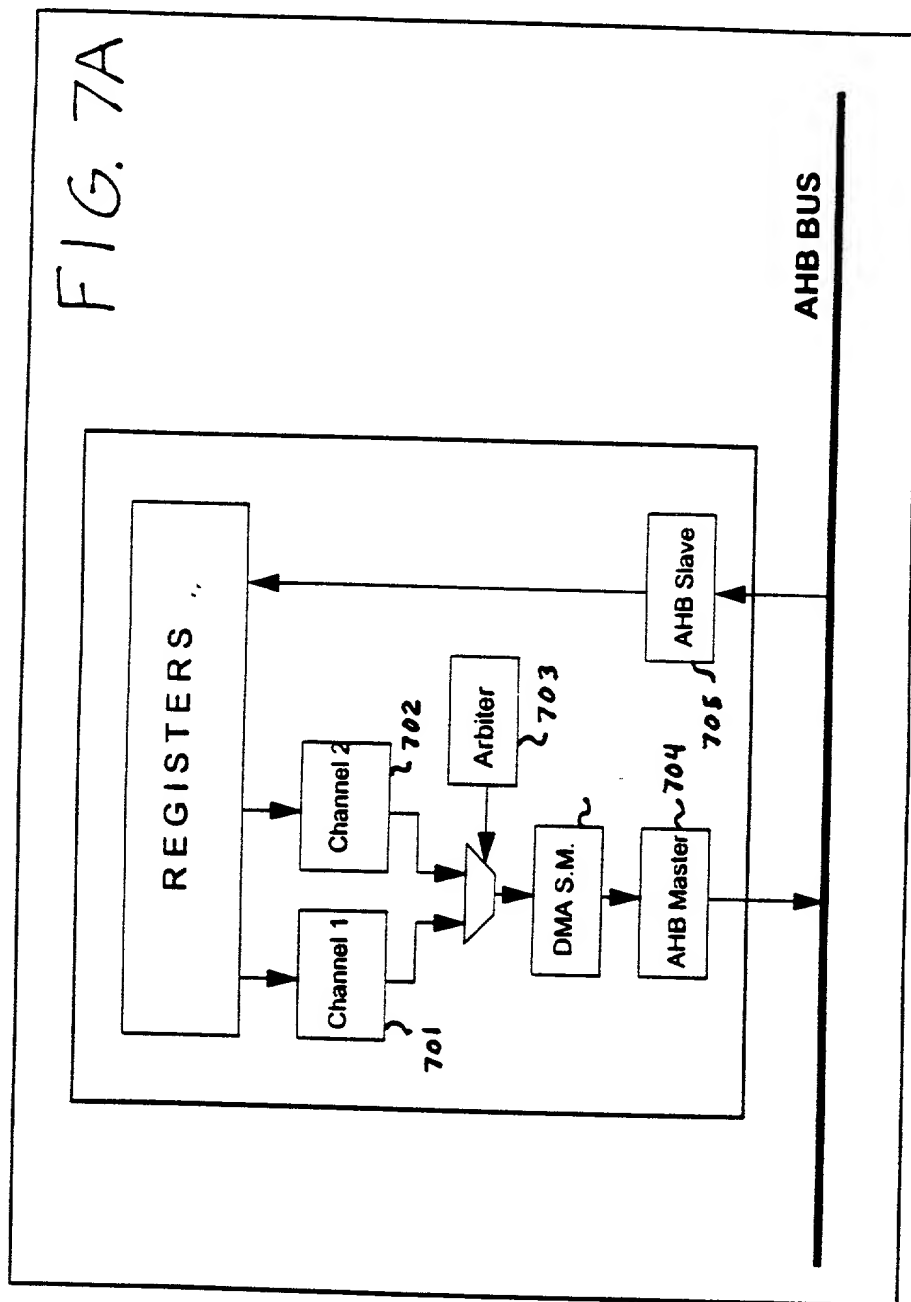


FIG. 7B

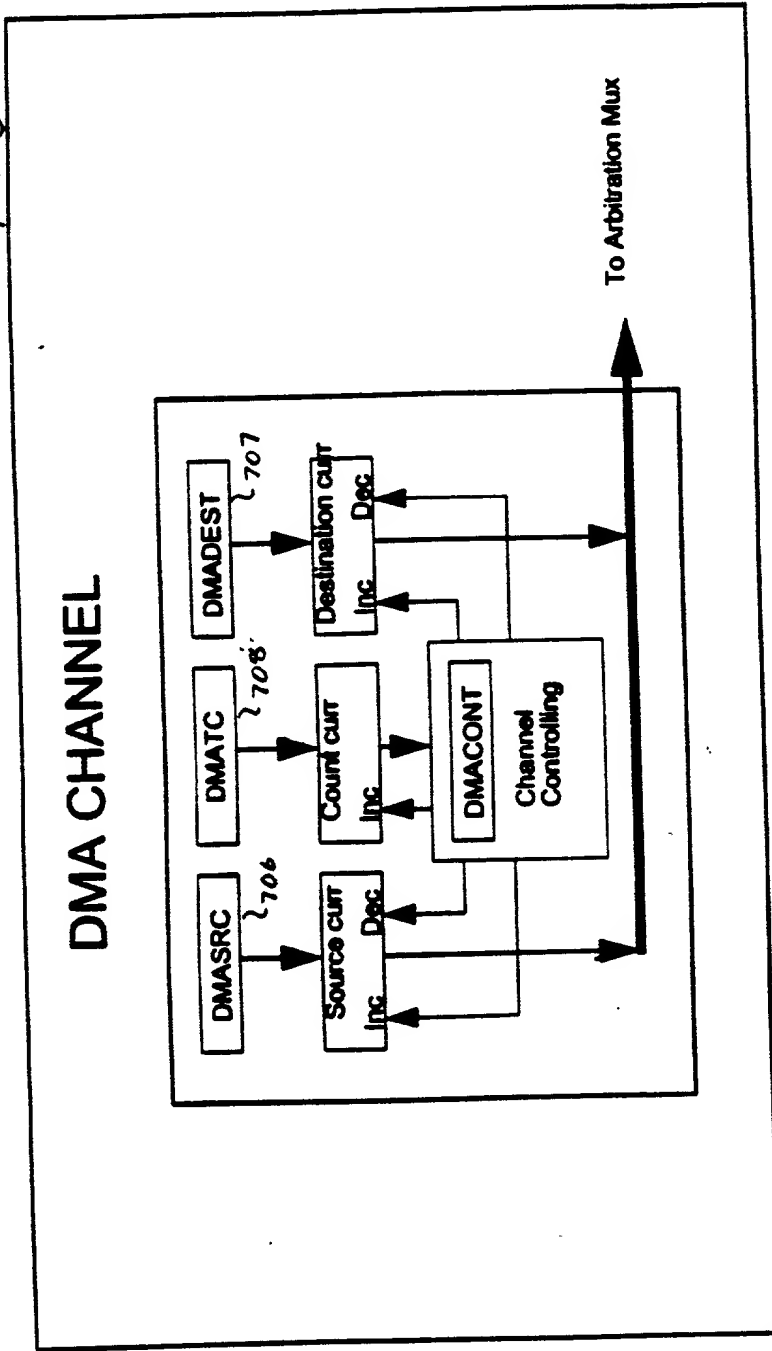
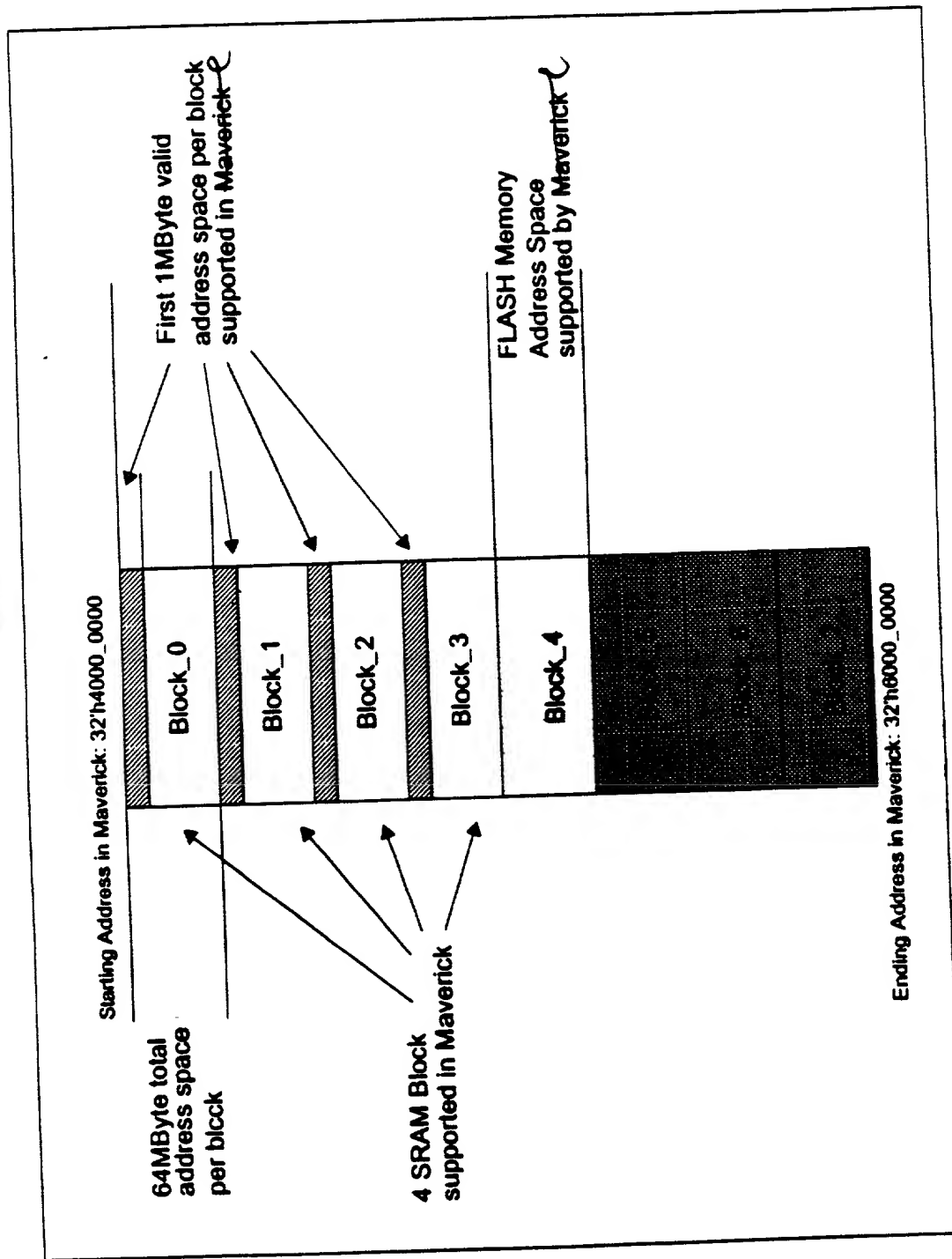
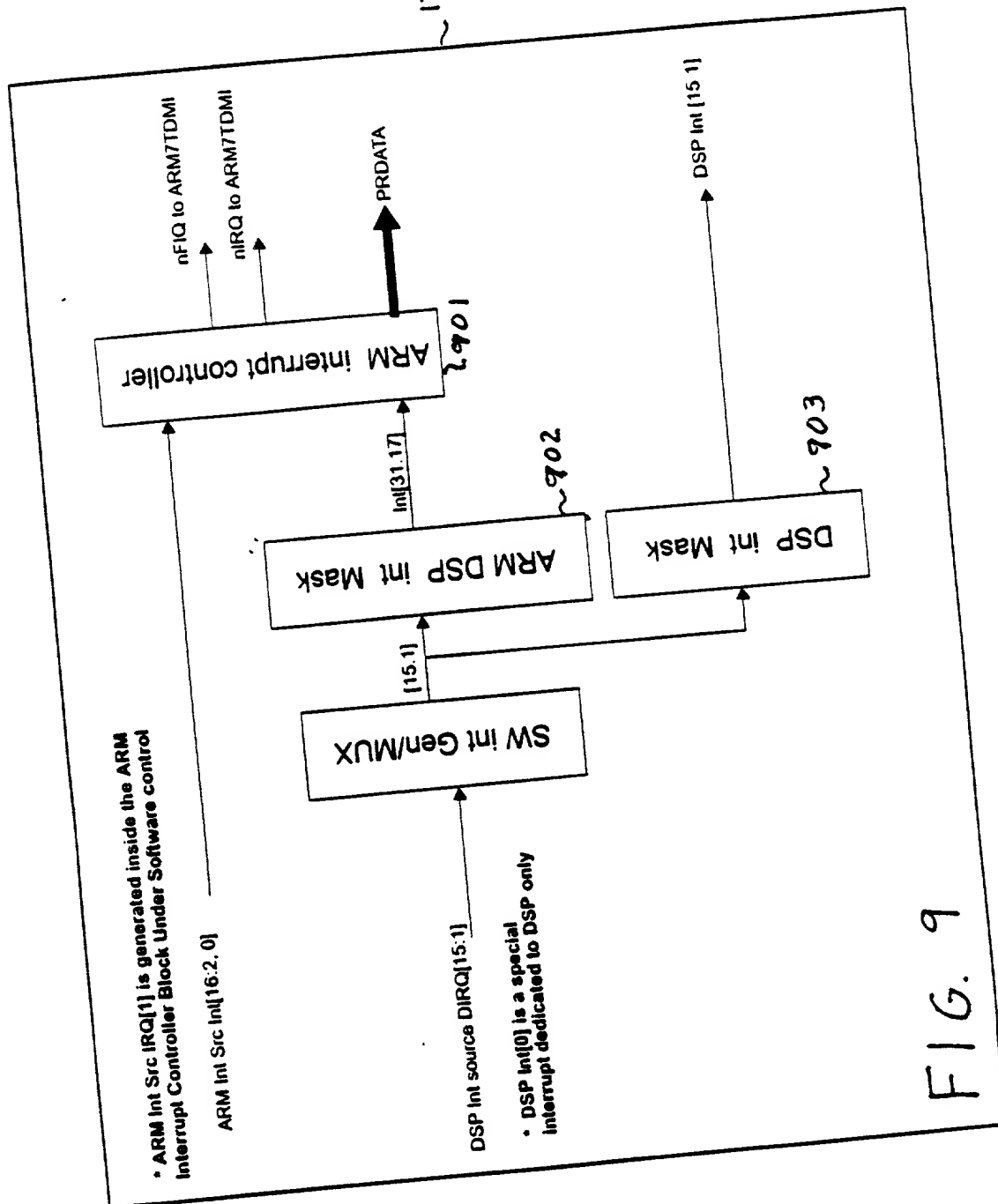


FIG. 8





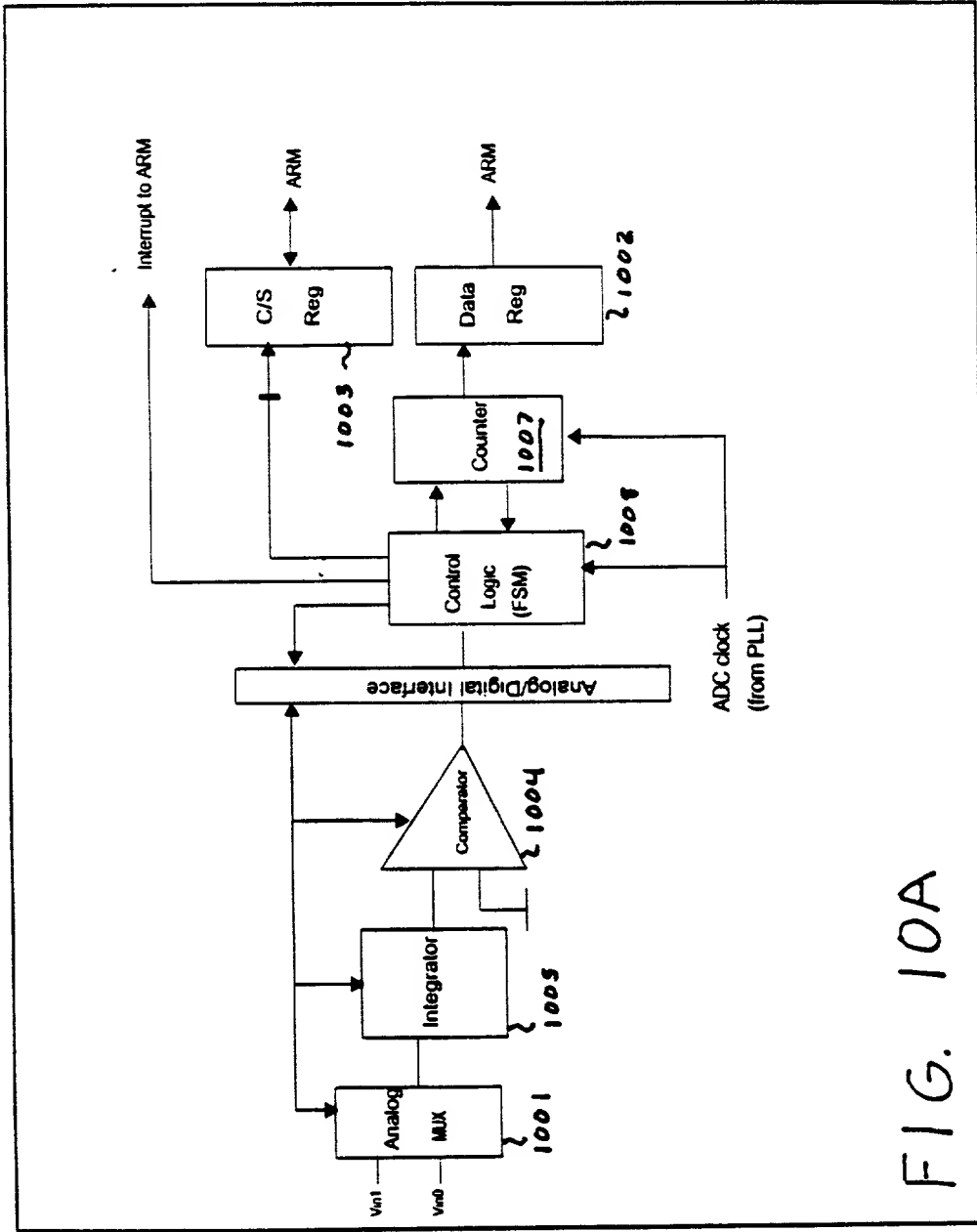


FIG. 10A

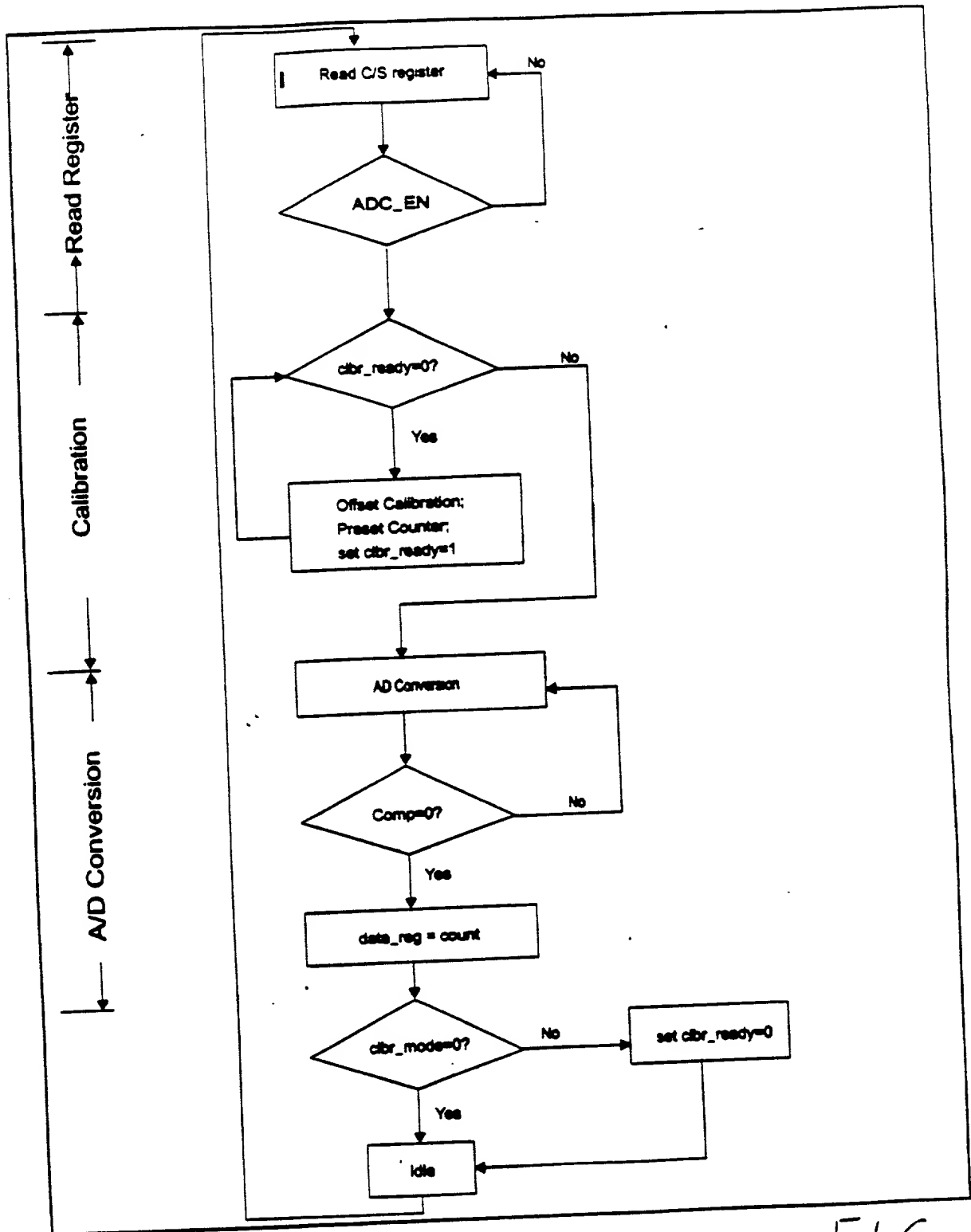


FIG. 10B

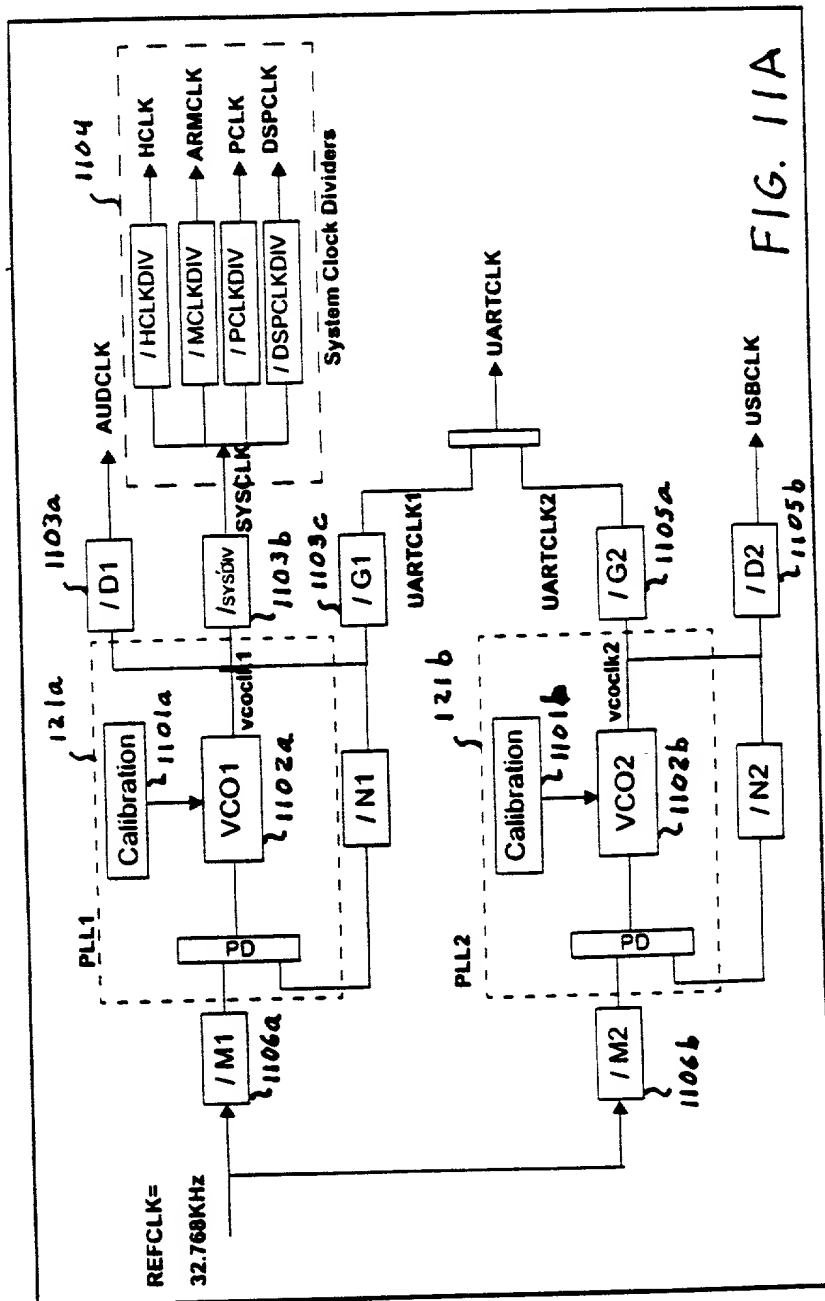


FIG. 11A

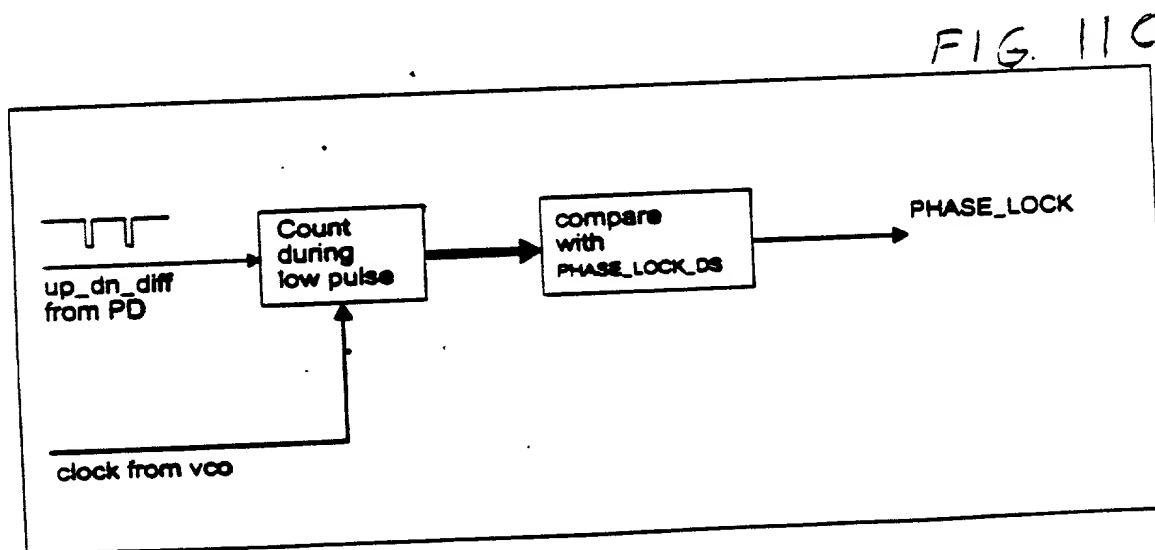
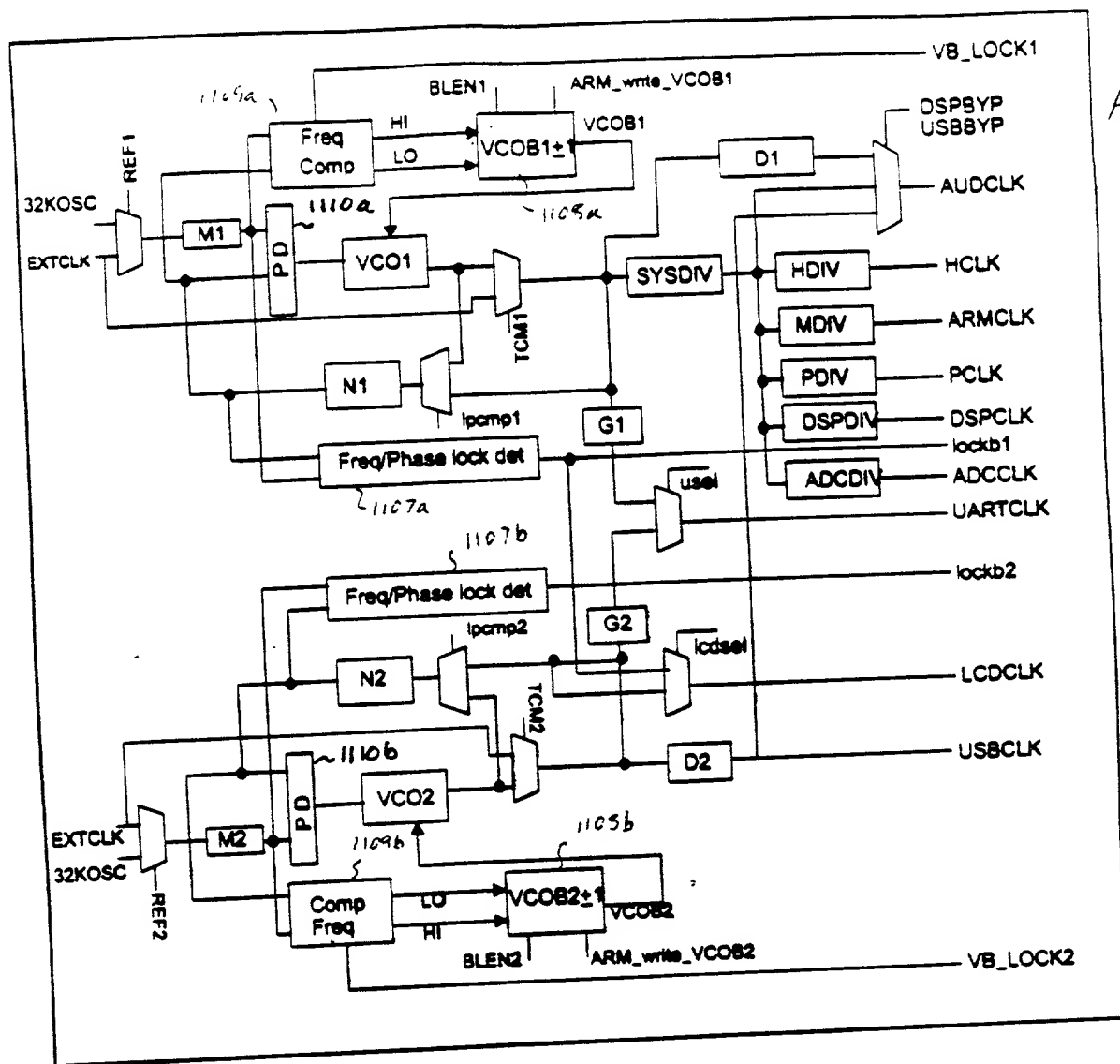
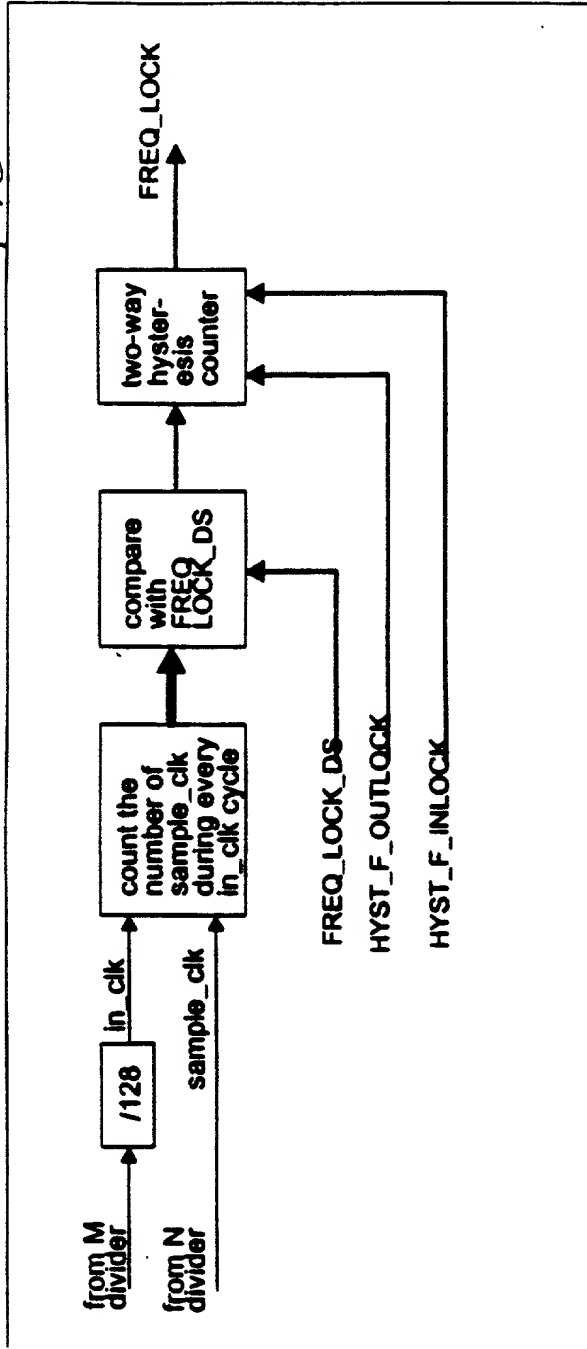


FIG. 11D



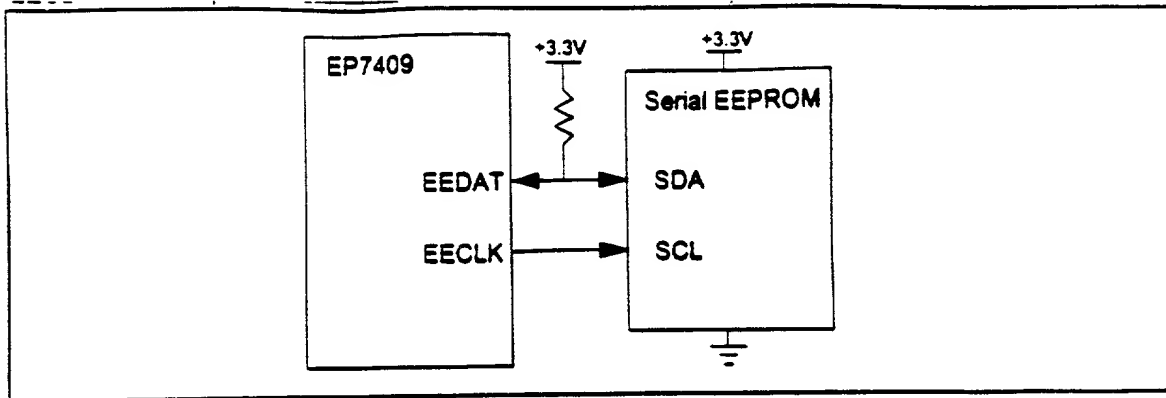
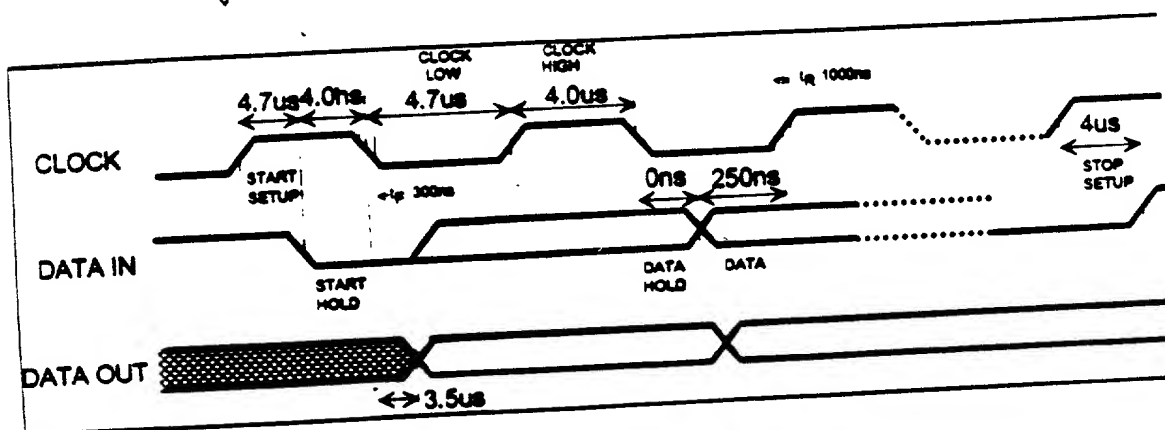
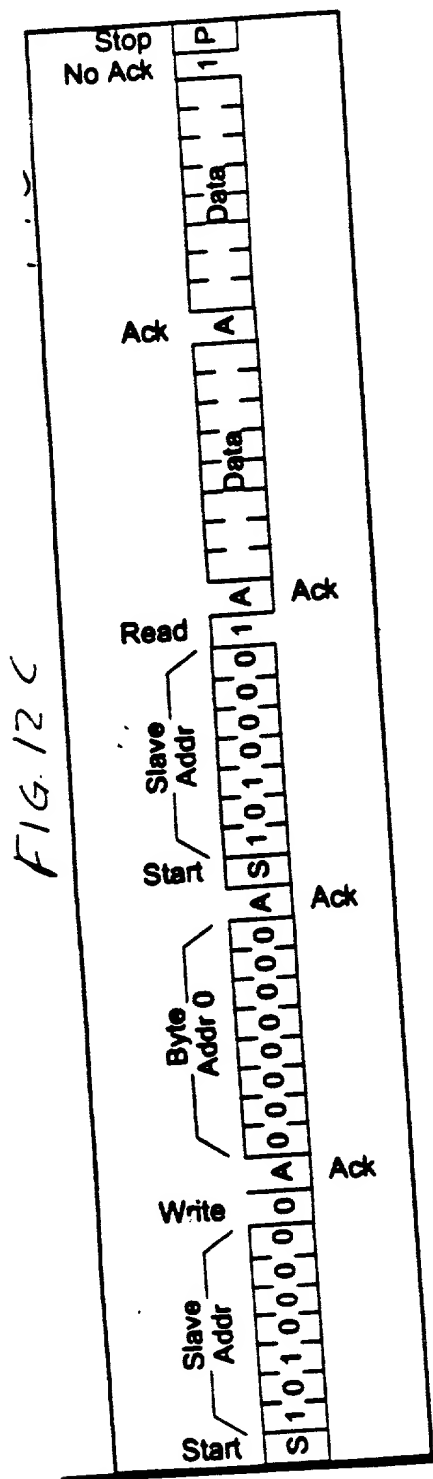


Fig. 12 A

Fig 12 B





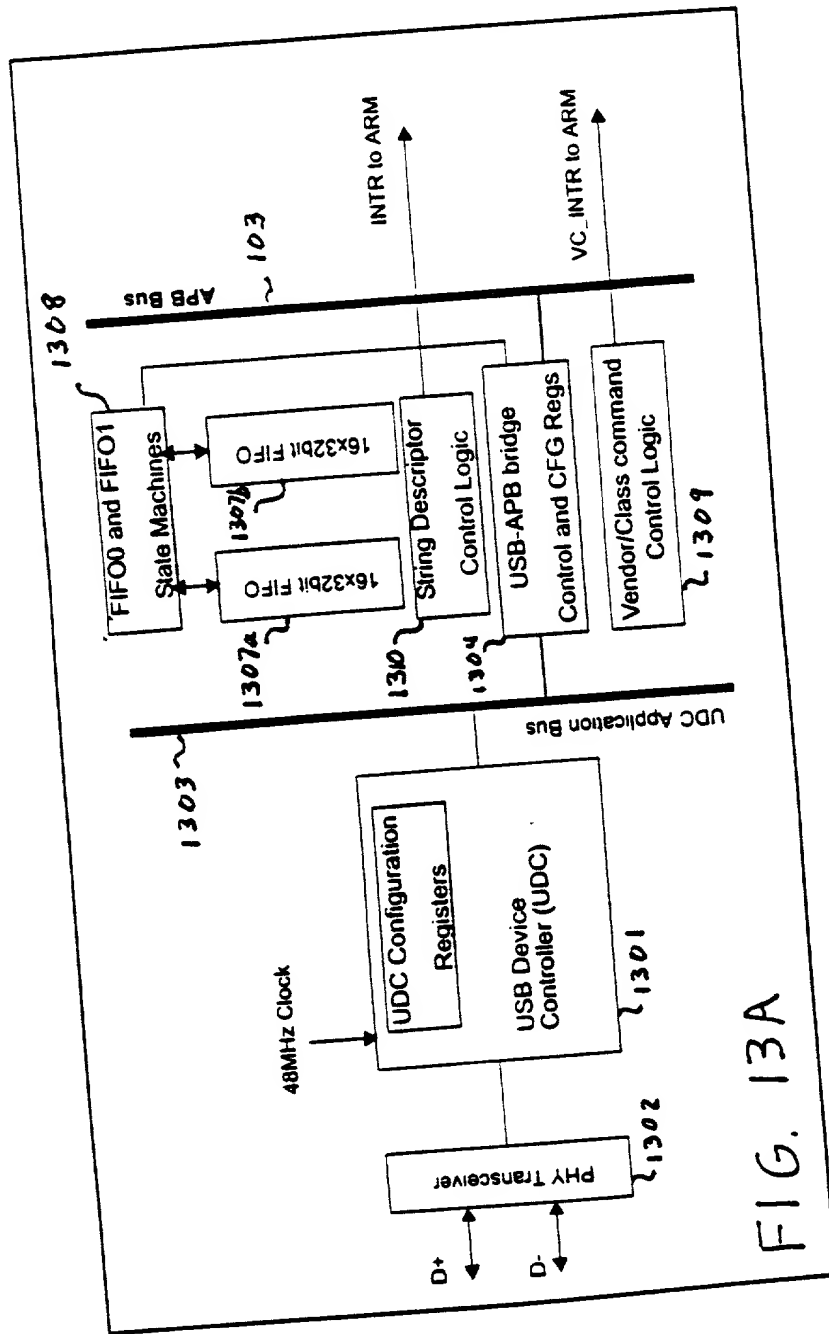


FIG. 13B

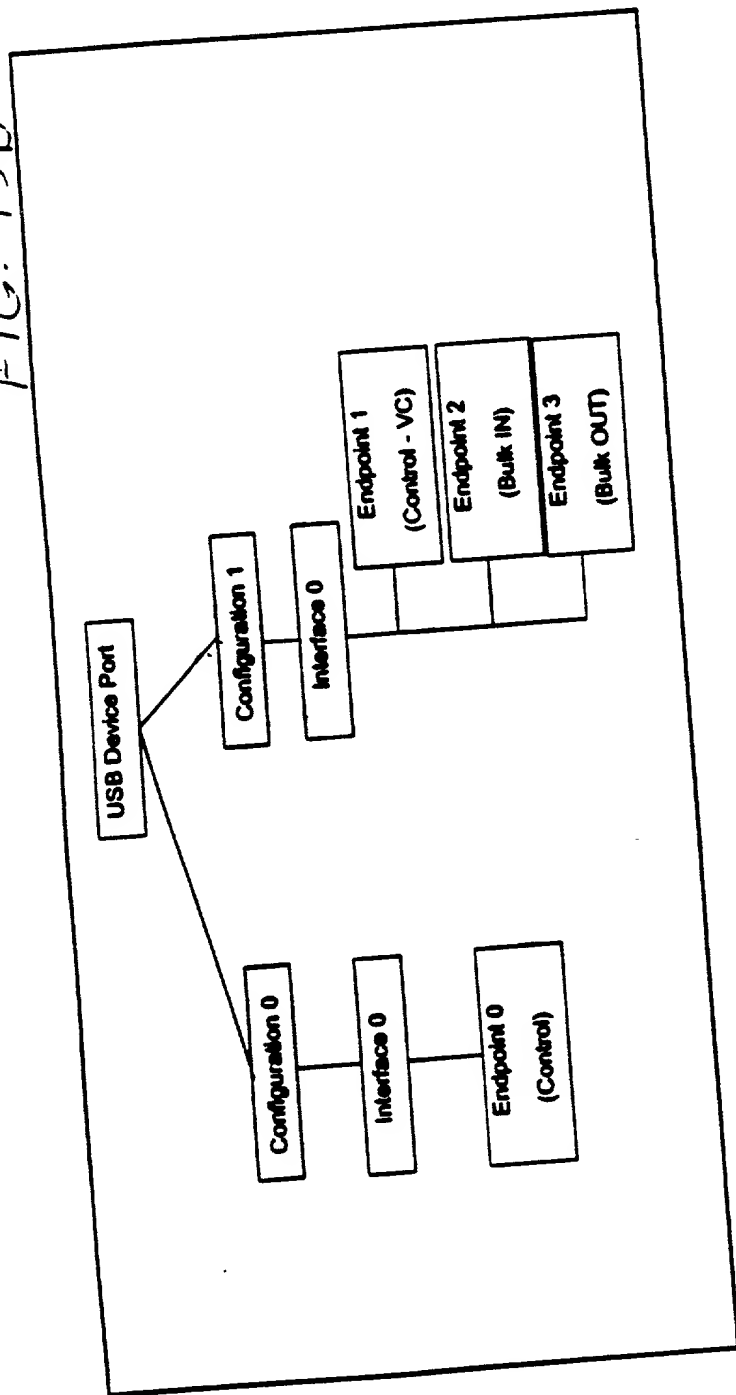


FIG. 14A

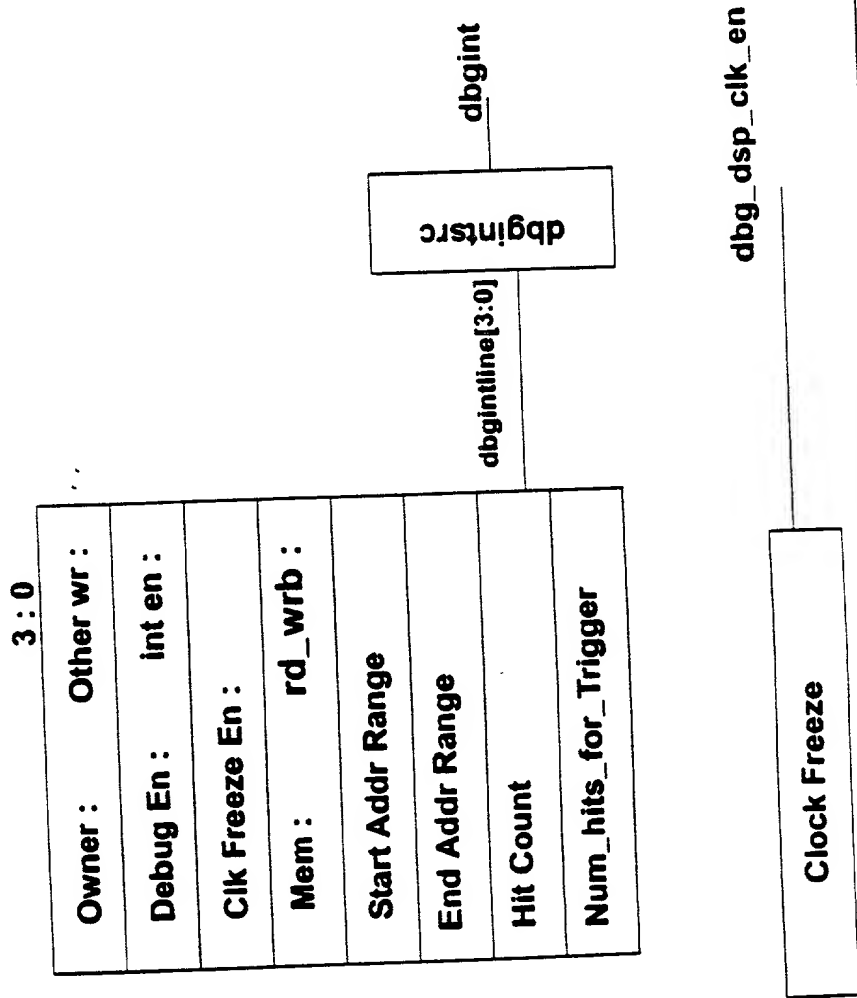


Fig. 14B

Sheet of 3

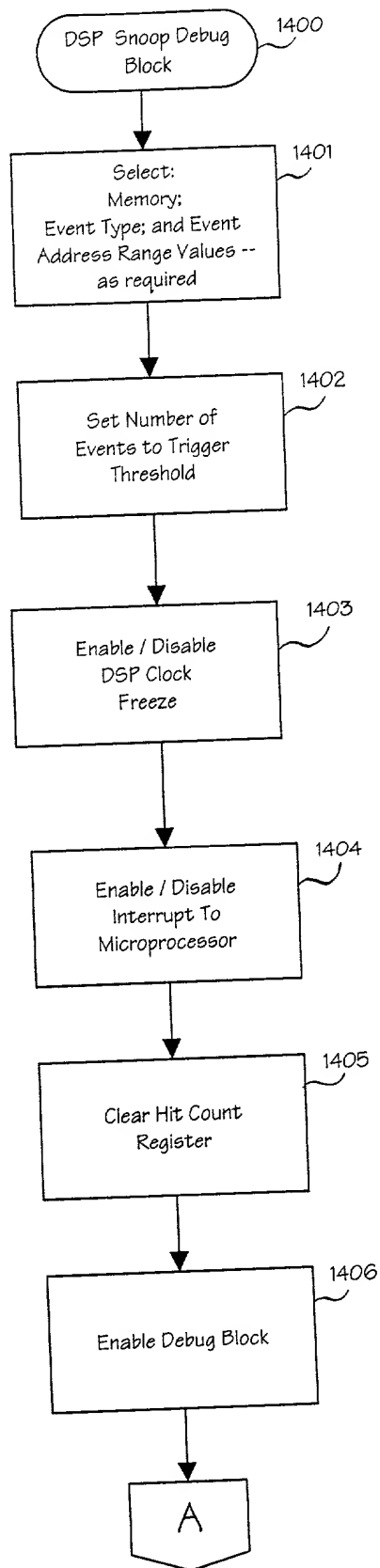


Fig 14B
Sheet 2 of 3

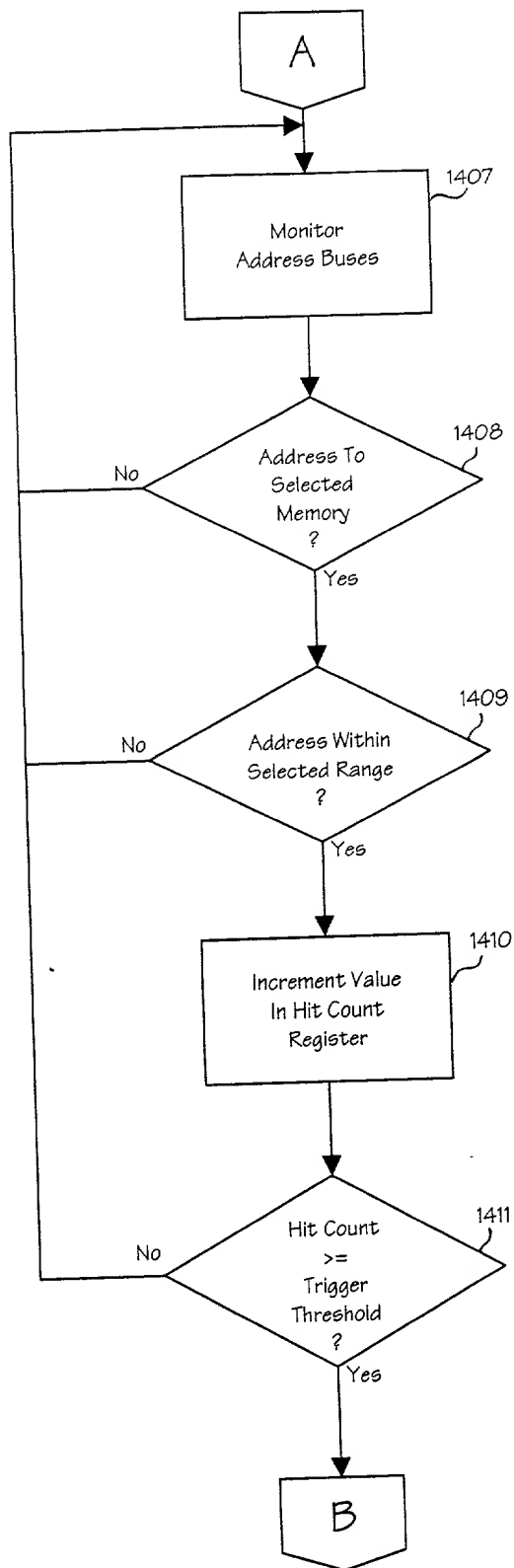
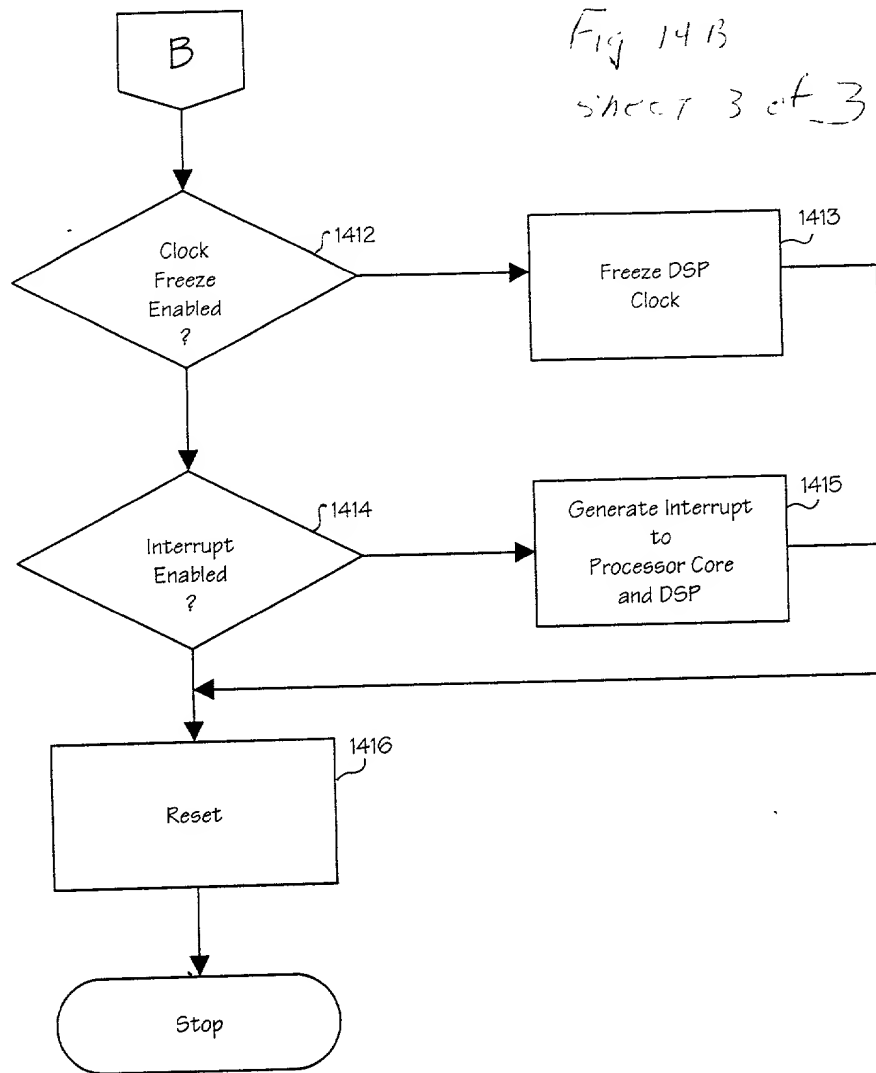


Fig 1413
sheet 3 of 3



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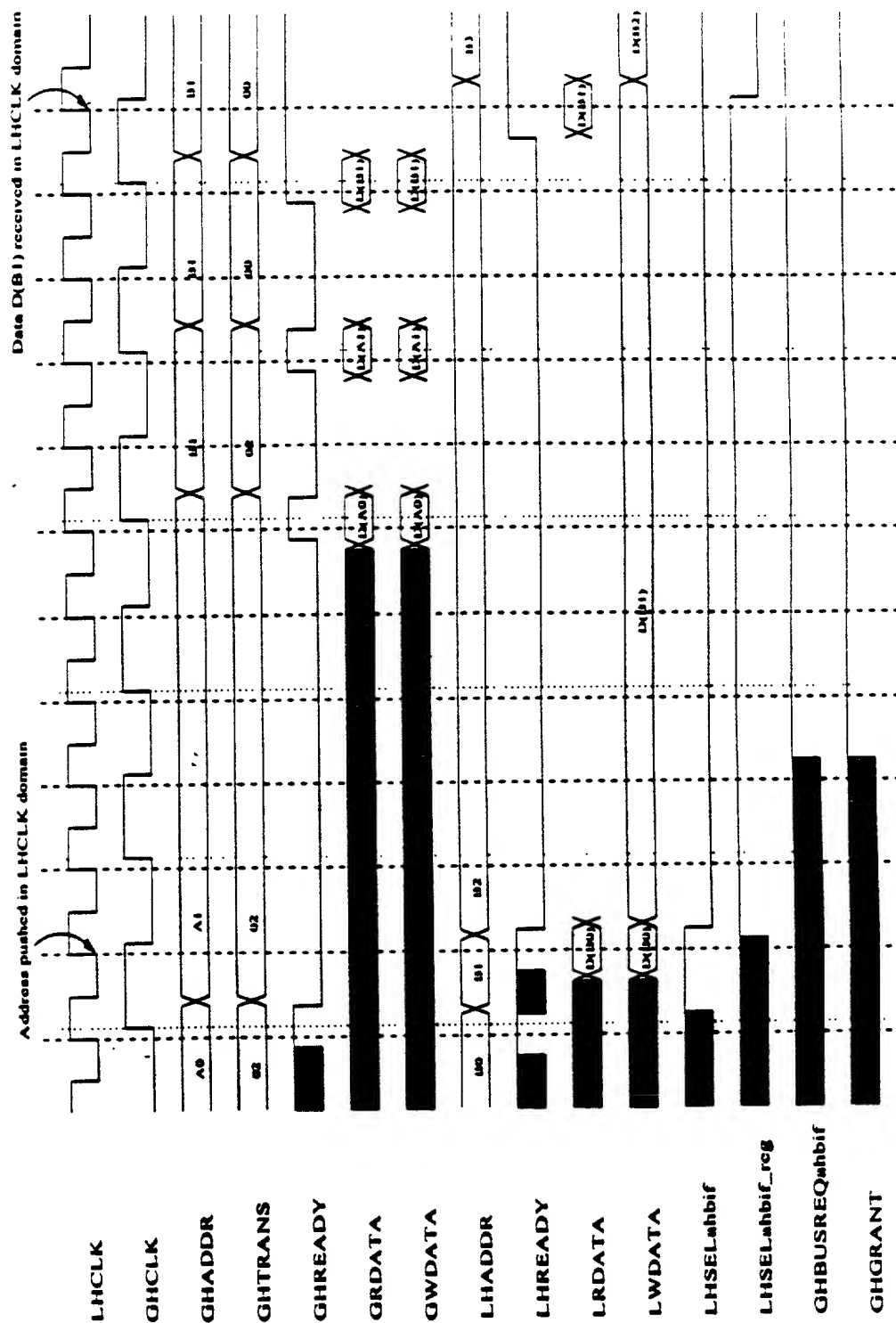
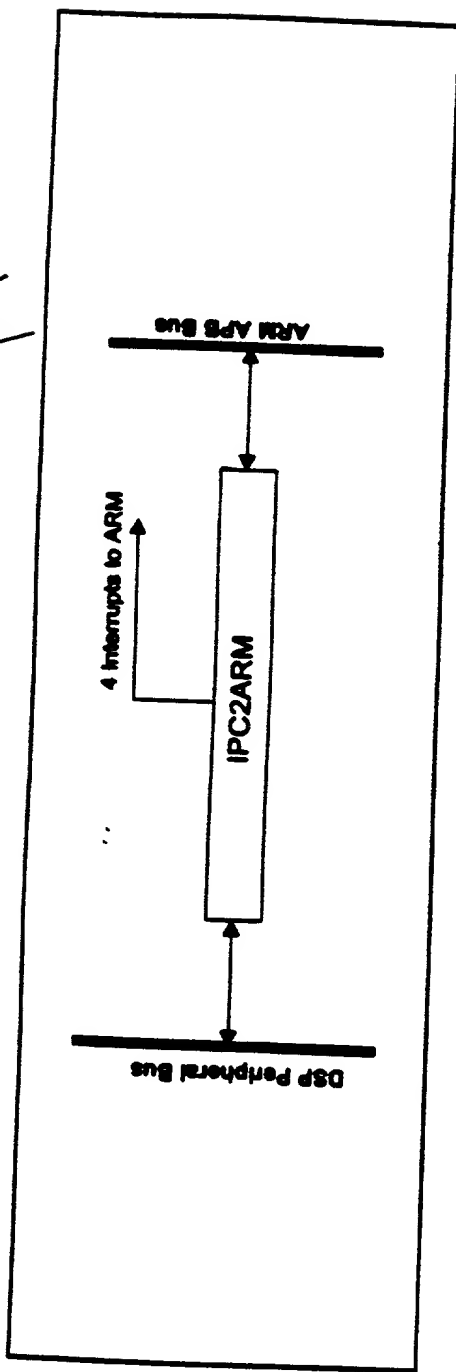


FIG 2D

FIG. 15



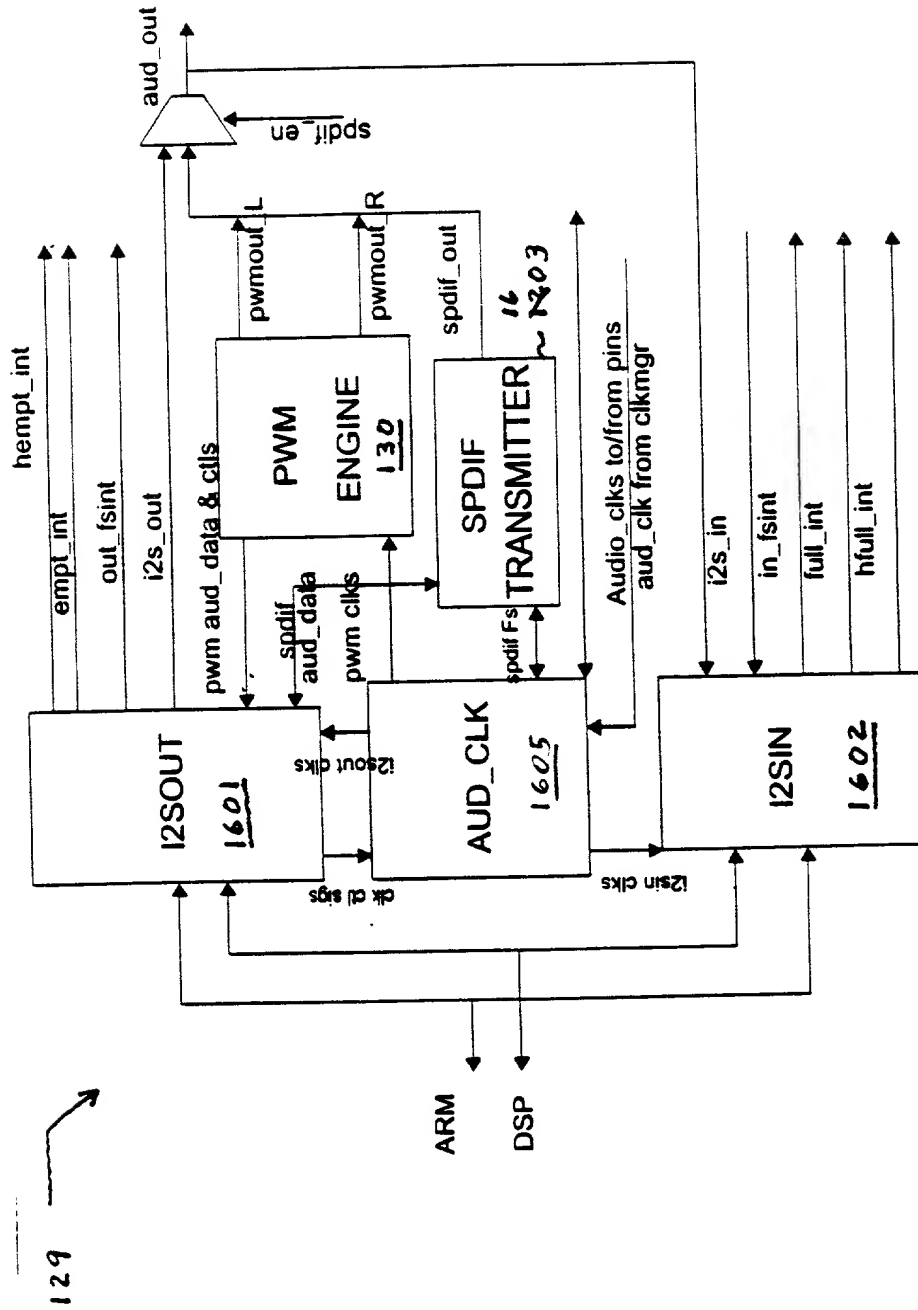


FIG. 16A

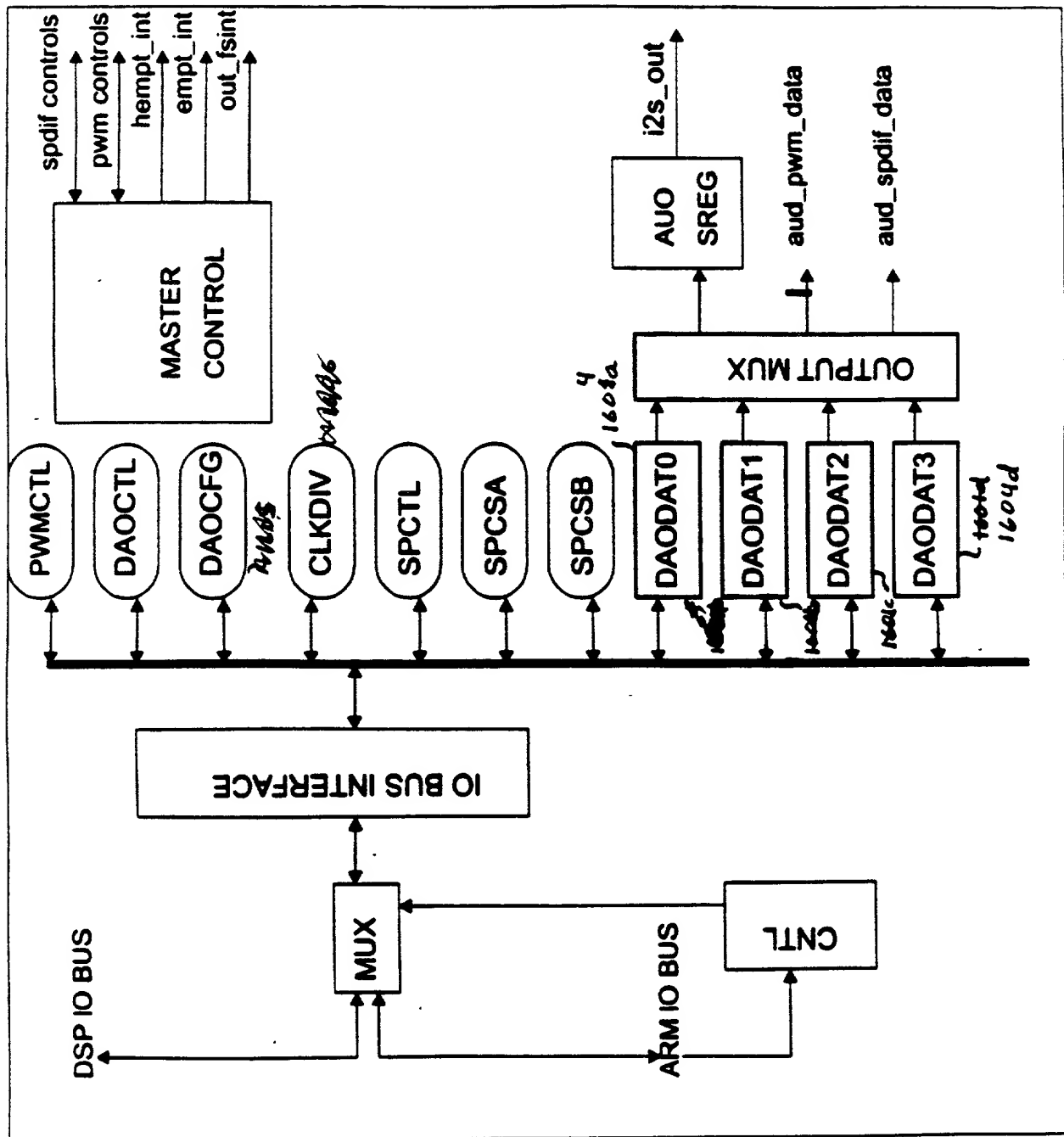


FIG. 16B

FIG. 16C

The following figure shows a typical output waveform.

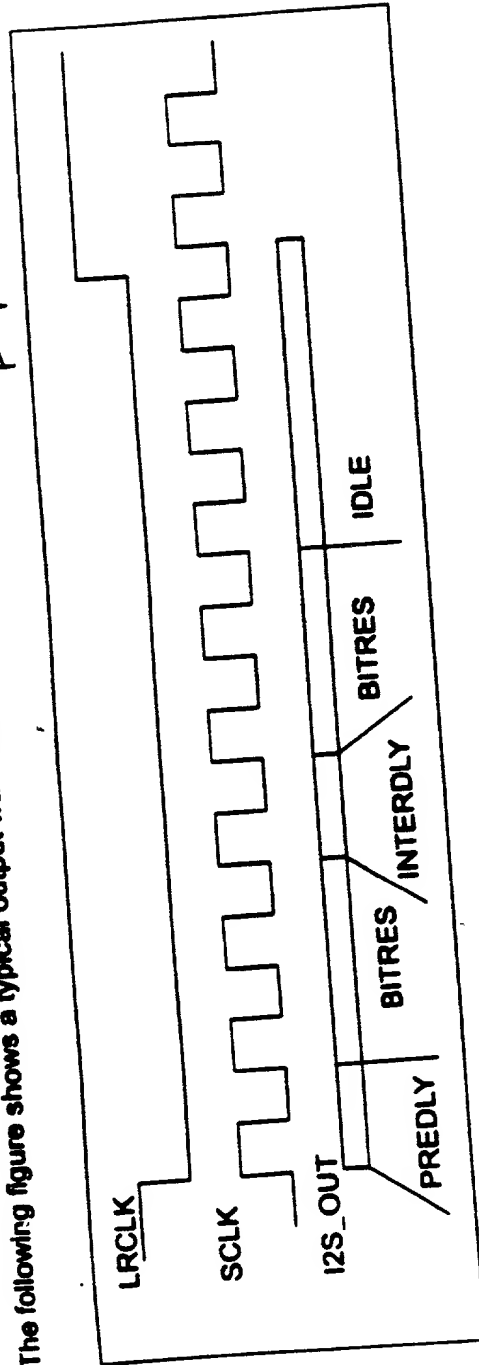


FIG. 16D

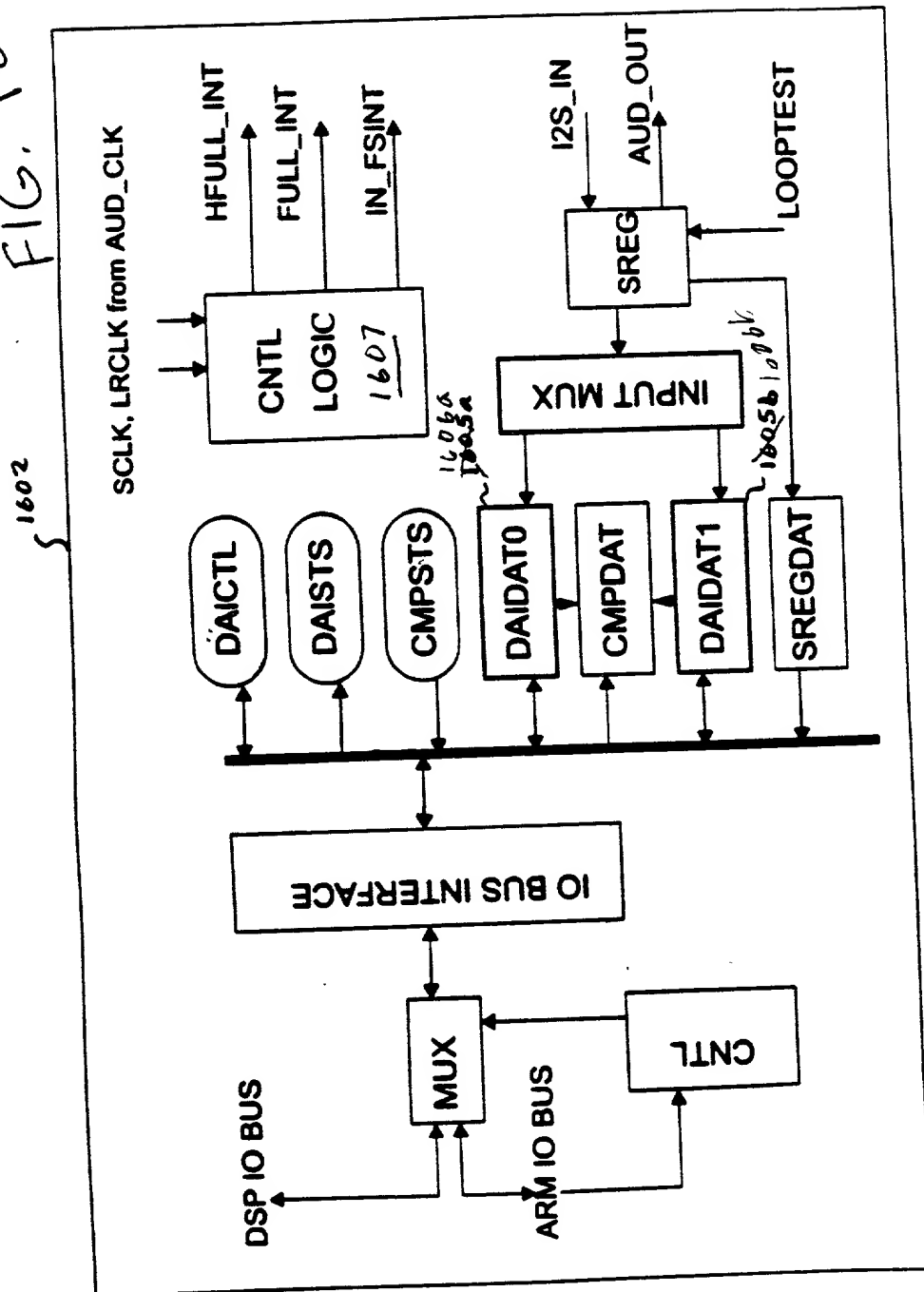


FIG. 17

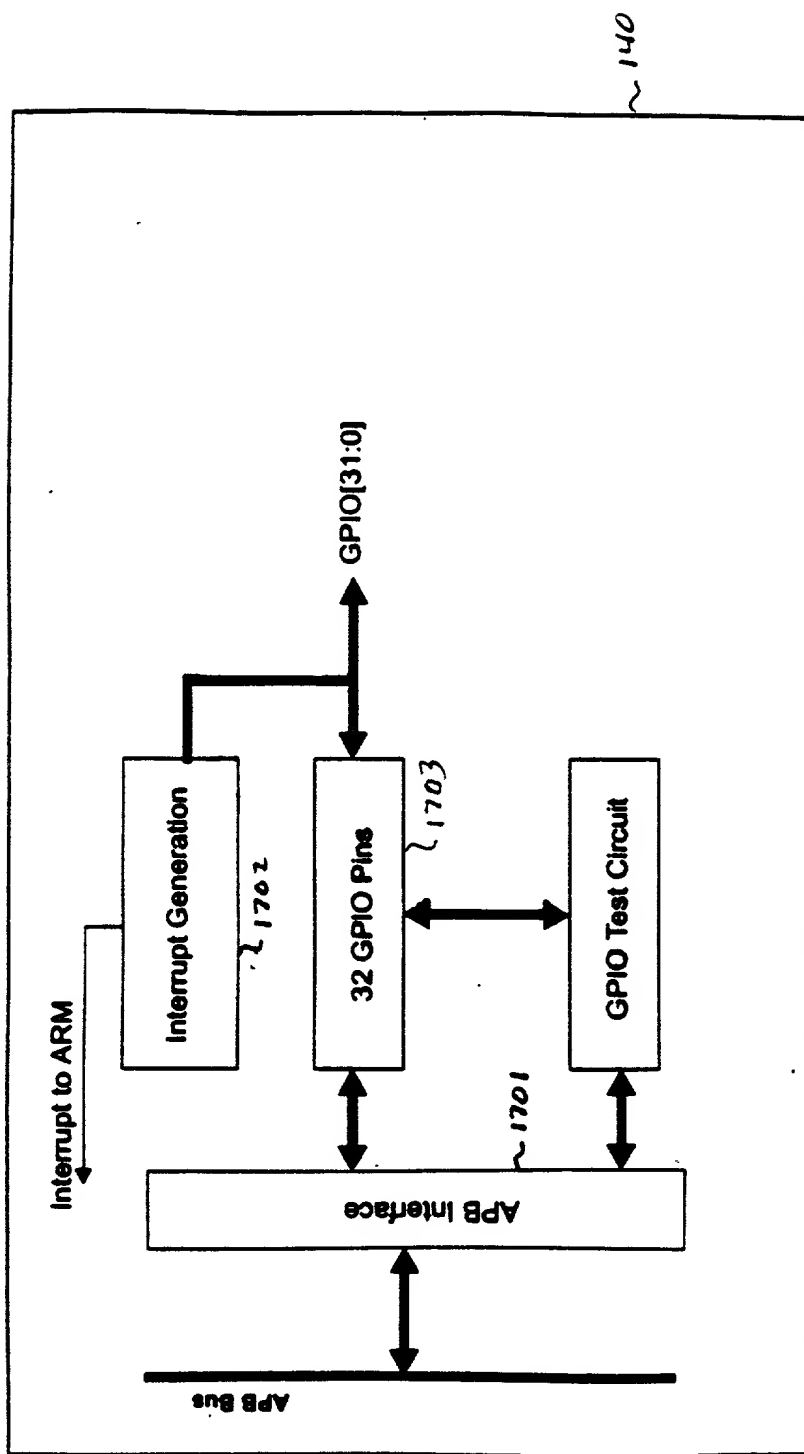


FIG. 18

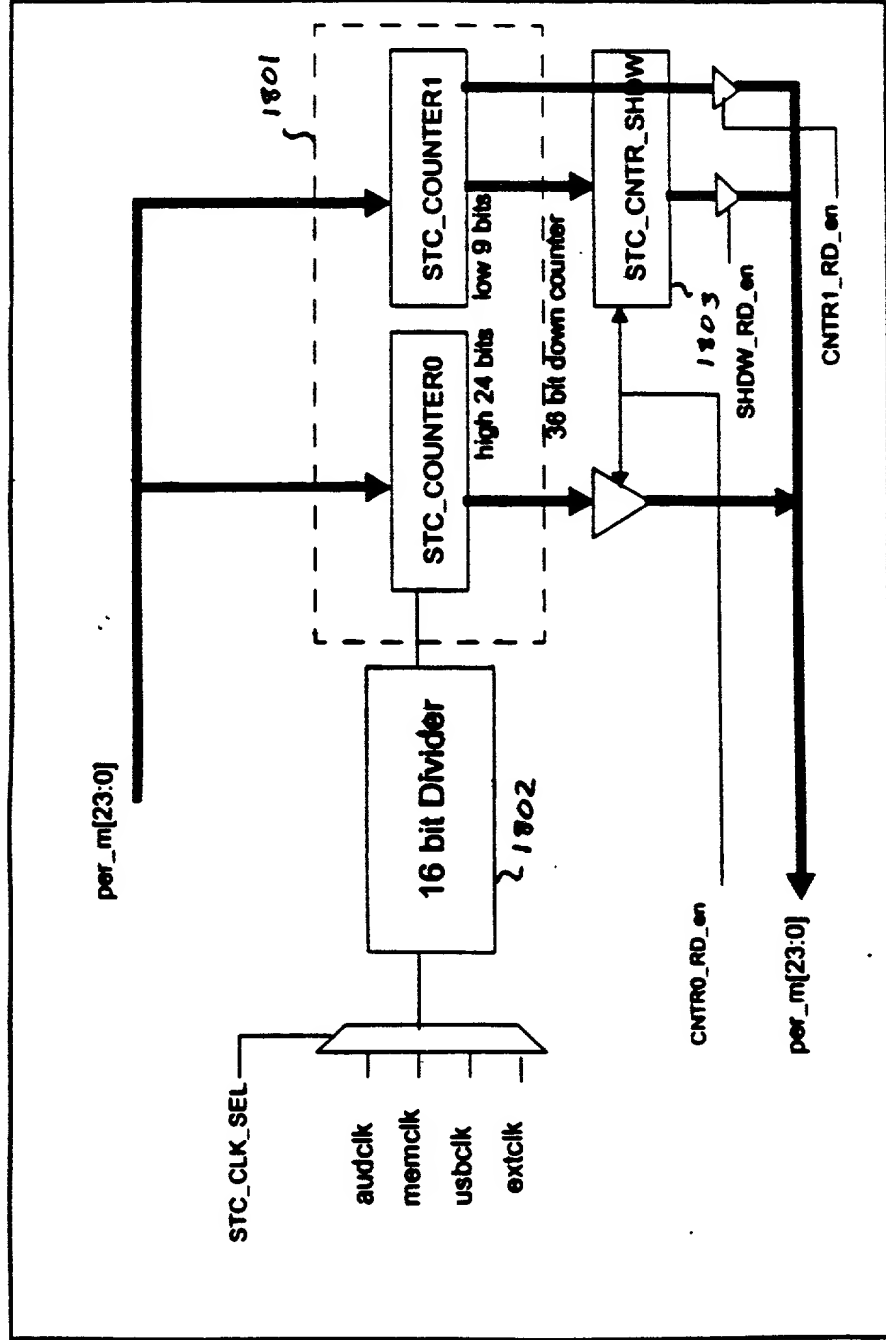


FIG. 19A

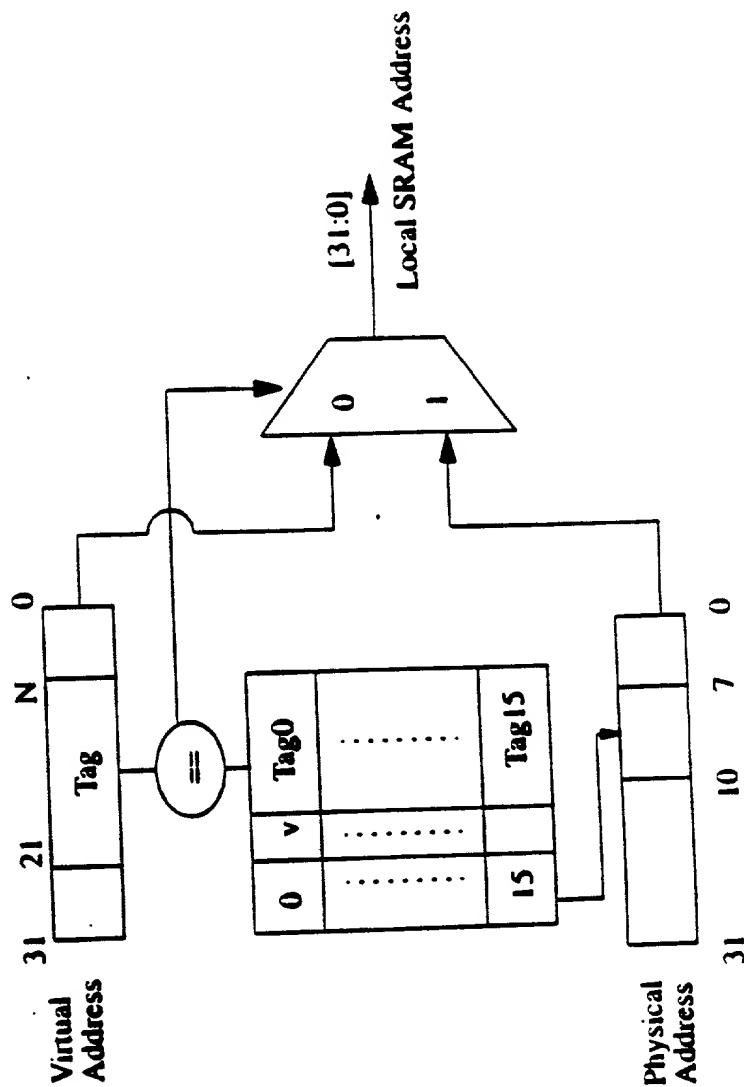
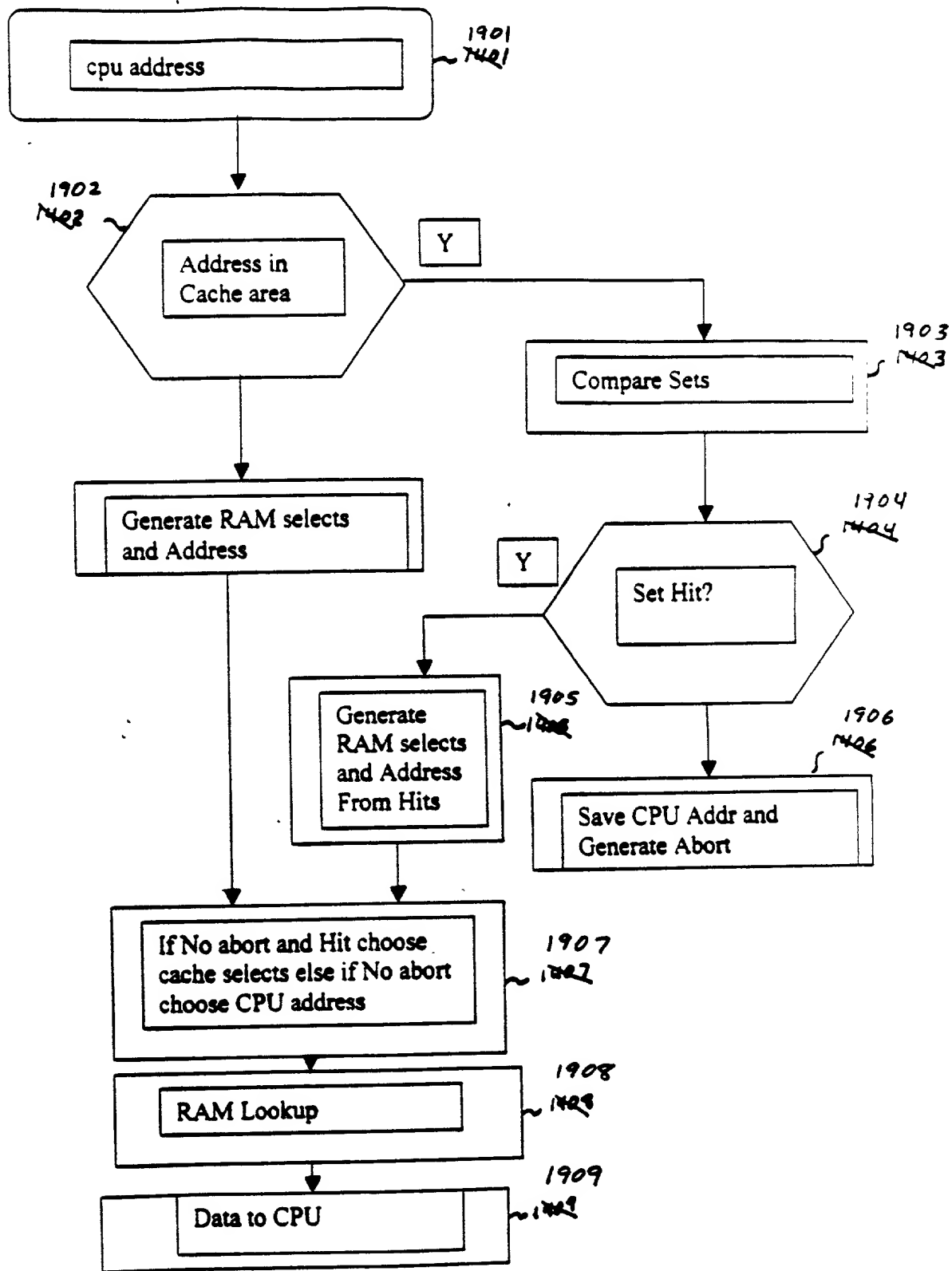


FIG 19B



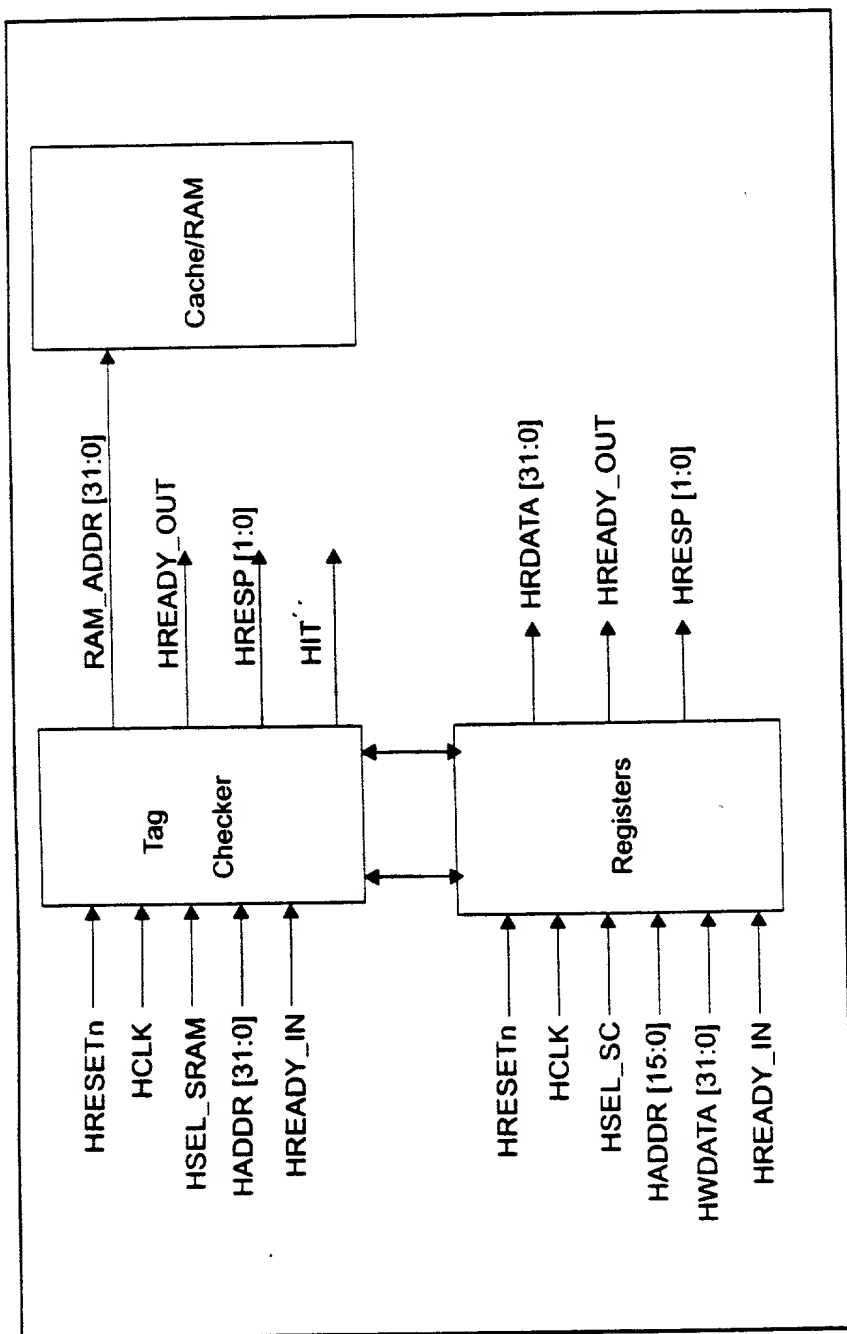


FIG. 19C

Fig. 20A

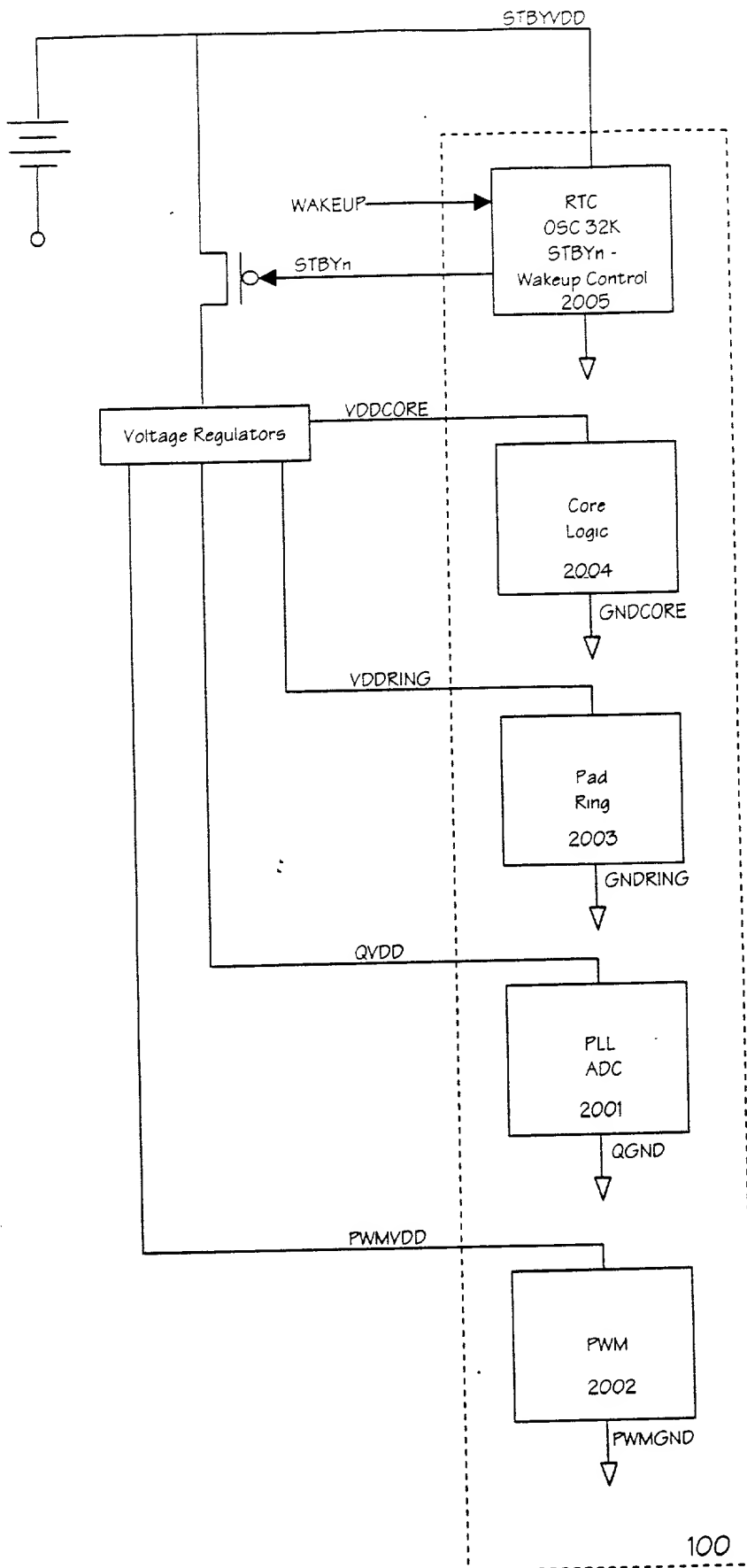


FIG. 20B

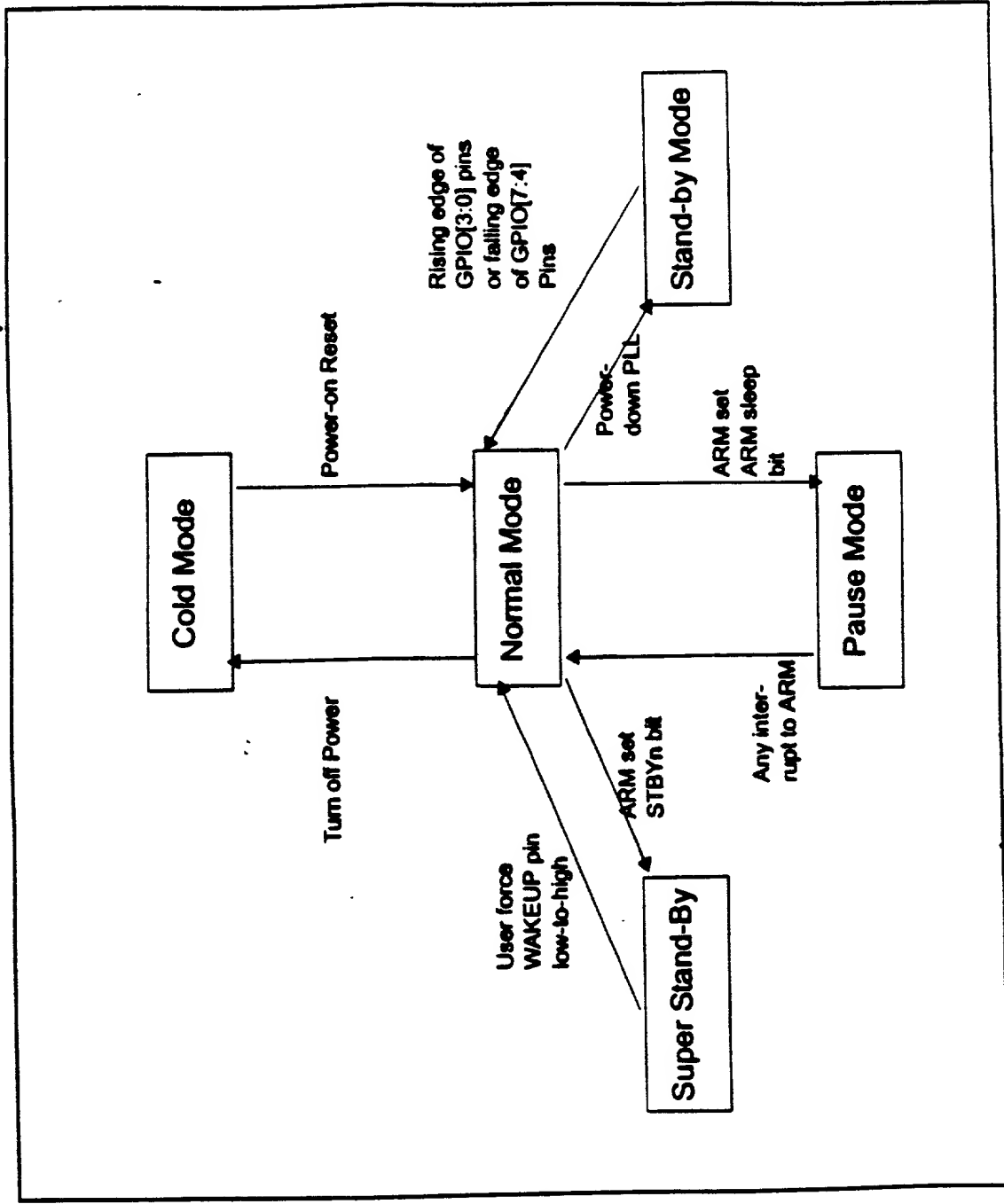


Fig. 20 C 5
Sheet 1 of 3

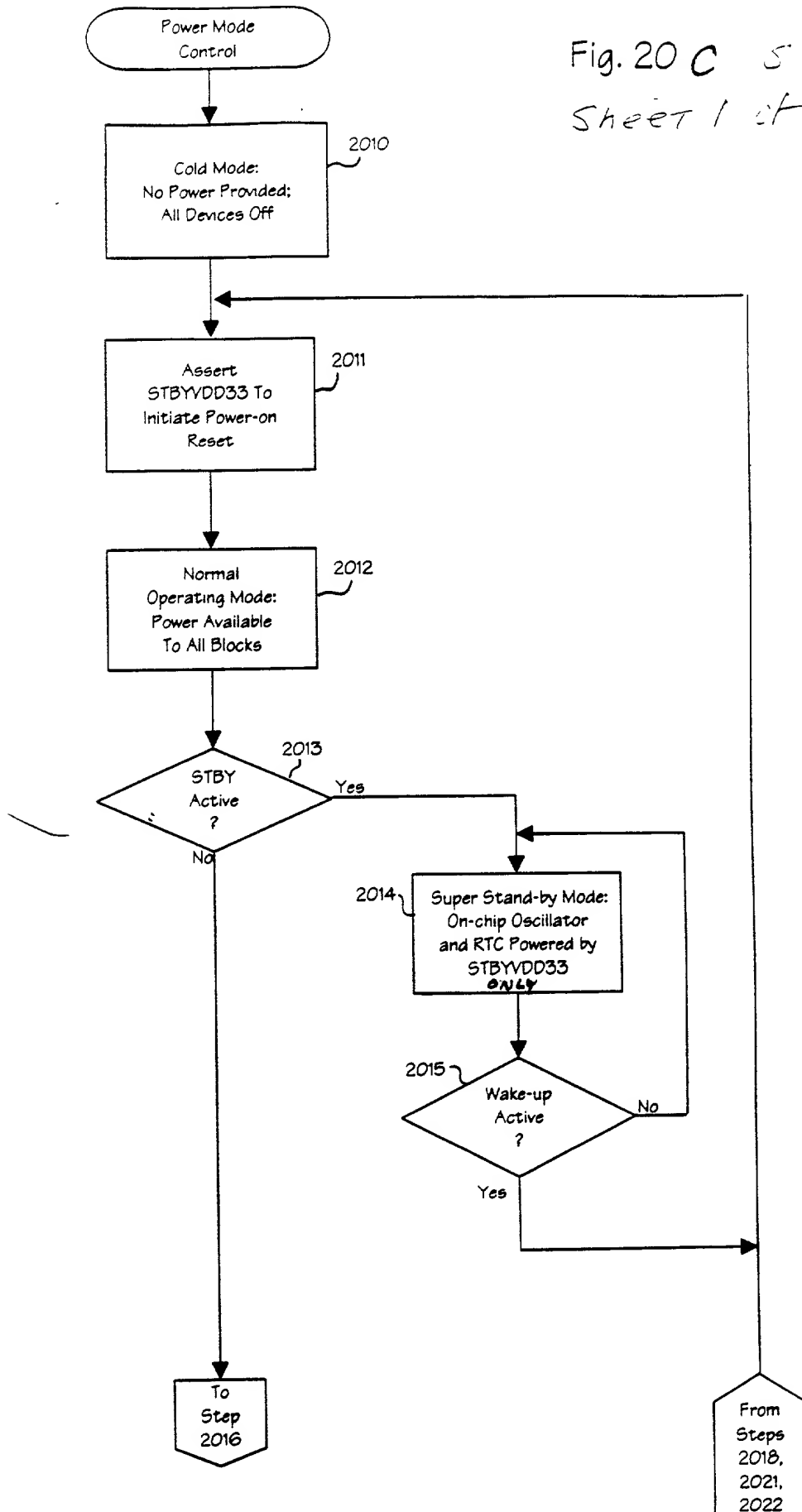
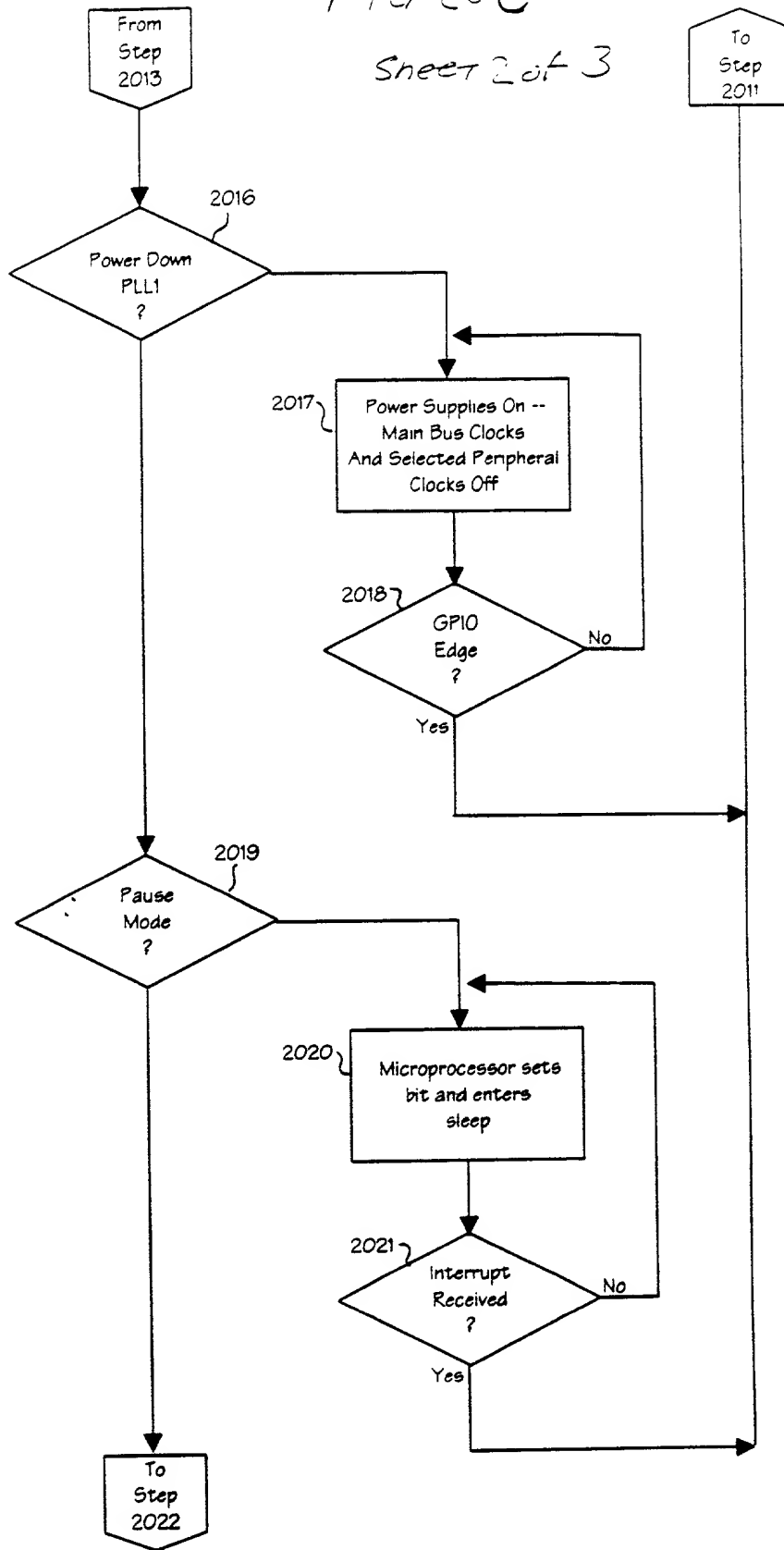


FIG 20C
Sheet 2 of 3



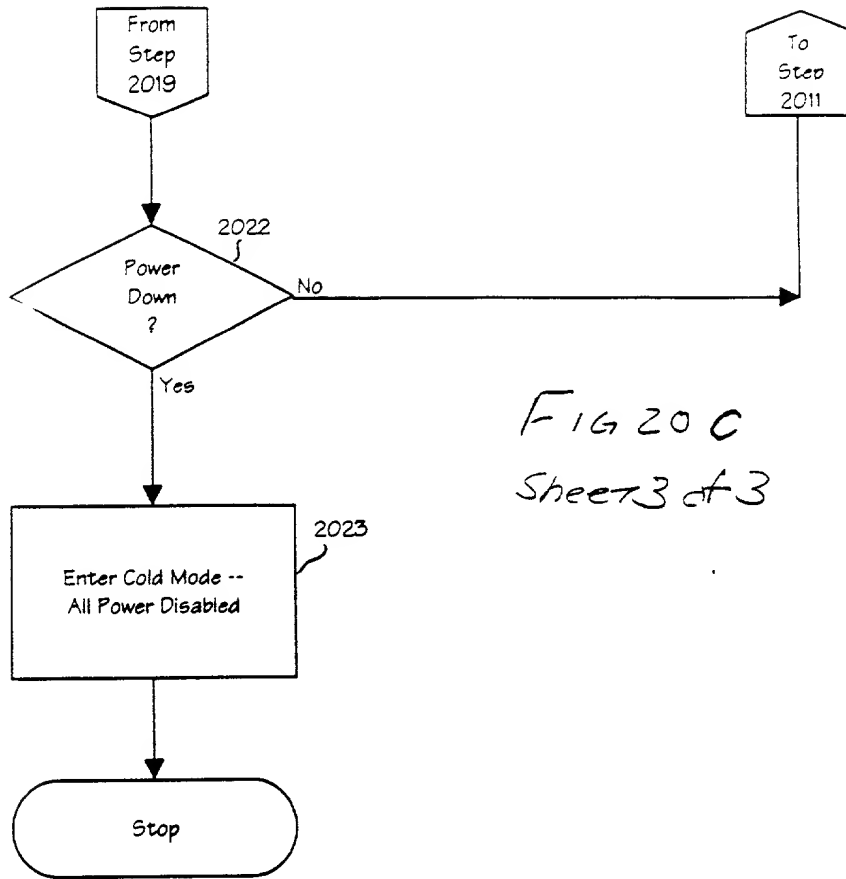


FIG 20C
Sheet 3 of 3

FIG 20C Sheet 3 of 3

